Advanced Micro Devices

The Am2900 Family Data Book

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LIST OF CHANGES

Listed below are changes incorporated in this data book relative to earlier editions of these data sheets.

Am2901

1. RO/LI and LO/RI dropped from shift pins. The shift pins are renamed RAM_0, RAM_3, Q_0, and Q_3.
2. All references to left and right eliminated.
3. Figure 4 revised for clarity.
4. Figure 8, line 7 corrected.
5. Flat pack dimensions and pin-out added.
6. $\overline{G}$ added to V_{OH} spec at -1.6mA I_{OH}.
7. Delays from D inputs in logic mode added to Table II.
8. Input/output circuits added.
9. Burn-in diagram added.

Am2905

1. AC data specified over operating range.

Am2906

1. AC data specified over operating range.

Am2907

1. AC data specified over operating range.

Am2909

1. AC data specified over operating range.

Am2911

1. New data sheet. Added to Am2909 data sheet.

Am2918

1. I_{CC} max. lowered from 130mA to 120mA.

Am29720/721

1. Part number changed from Am2950/51.

Am29760/761

1. Part number changed from Am2970/71

Am29790/791

1. Part number changed from Am2980/81.

INTRODUCTION

THREE GENERATIONS OF TTL

Transistor-transistor logic has been the dominant technology for digital circuits since it was developed in the mid-1960's. It has proven itself to be manufacturable in high volume using an extremely reliable process technology. The processes used for TTL have evolved over the years, making components smaller, faster and less expensive. Relative to a TTL gate manufactured in 1966, a gate on a circuit manufactured today occupies 1/5 the area, consumes 1/10 the power, is twice as fast and costs less than 1/100 the price.

The circuits built using TTL technology have gone through two generations; the Am2900 Family represents the beginning of the third. Each generation consists of circuits which are fundamental building blocks of systems – circuits which can be interconnected in many different ways to build many different systems. Only by producing such universal circuits can manufacturing volumes be high enough to generate the rapid cost reductions characteristic of the integrated circuit industry.

The quality which distinguishes one generation from another is the level of integration used, and, because of the level of integration, the philosophy behind the circuit.

If one draws a curve plotting the cost of an individual gate against the number of gates on a chip, Figure 1 results.

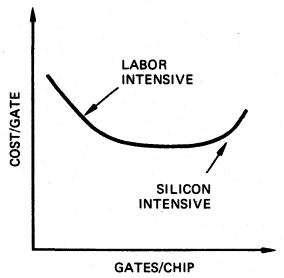


Figure 1.

At the left, cost per gate is inversely proportional to the number of gates on the chip. The chip is small enough that it does not represent a significant portion of the cost of the product – it is virtually free. The cost of the product is composed of labor in assembly and test, the cost of processing an order, shipping and fixed overhead. Doubling the number of gates on the chip doesn't materially affect the cost so the cost per gate halves. As the number of gates per chip increases, the die begins to cost more, reversing the downward trend. As die cost dominates, the cost per gate remains relatively flat until the yield of the die begins to decline markedly. The cost per gate then begins to rise again. The lowest cost per gate is achieved at a level of integration corresponding to the flat region. This is the optimum level of integration.

As technology improves, costs are constantly reduced and the optimum level of integration occurs at more and more gates per chip.

The three curves of Figure 2 are the reason for the three generations of TTL. Each generation has consisted of fundamental system building blocks designed to take advantage of the optimum level of integration at the time.

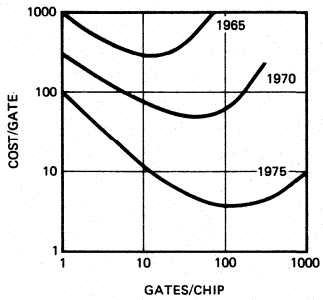


Figure 2.

GENERATION I – SSI, 1965

In 1965, the optimum level of integration was three-to-six gates per chip. Users were delighted to buy such chips at $10–20 each. The circuits were useful in many systems. They consisted of gates – the 7400, 7410, 7420 – and, pressing the state of the art, some flip-flops. They were fundamental building blocks.

GENERATION II – MSI, 1970

Beginning around 1968, it became economical to put more gates on a chip and the industry was faced with a problem: How does one put 20 gates on a chip and build a universal building block? Clearly, one answer was to bring the inputs and outputs off chip as had been done before. But that was the wrong answer. The right answer was to redefine fundamental building blocks. The new building blocks fell into seven categories:

- Counters
- Decoders
- Multiplexers
- Operators (adders, comparators)
- Encoders
- Registers
- Latches

All systems could be defined in terms of these seven functions, and integrated circuits could be defined at the 20–50 gate/chip level which performed these functions efficiently. This, of course, is MSI. Over the last six or seven years, more and more circuits of this type have been introduced, utilizing standard gold-doped technology, low-power TTL, high-speed TTL, Schottky TTL, and now low-power Schottky TTL technology. Today, there are over 250 different MSI circuits and new ones appear every month. But in today's technology, many of these circuits are not particularly cost effective. They are too small for today's technology and their costs are labor intensive. (Labor costs do not follow traditional semiconductor pricing patterns.) In 1976, the optimum level of integration for bipolar logic is around 300 gates/chip.

GENERATION III – The Am2900 Family, 1976

At a 300-gate-per-chip level of integration, one does not build counters, decoders, and multiplexers. A new definition of fundamental system functions is needed. Advanced Micro Devices has defined these eight categories:

- Data Manipulation
- Microprogram Control
- Macroprogram Control
- Priority Interrupt
- Direct Memory Access
- I/O Control
- Memory Control
- Front Panel Control

The Am2900 Family consists of circuits designed to perform those functions efficiently. They are fundamental system building blocks; they contain hundreds of gates per chip; they are fast – utilizing Low-Power Schottky TTL technology; they are expandable; they are flexible – useful in emulation; and they are driven under microprogram control.

Hello, LSI. Introducing the Am2900 Family.

THE Am2900 FAMILY

The Am2900 Family consists of a series of LSI building blocks designed for use in microprogrammed computers and controllers. Each device is designed to be expandable and sufficiently flexible to be suitable for emulation of many existing machines. It is the wide variety of machine architectures possible with the Am2900 Family which sets it apart from the fixed-instruction microprocessors such as the Am9080A.

While an Am9080A can be used to build a microcomputer with only four or five packages, an Am2900 design will require 30 or 40 or more. The Am9080A design will, therefore, almost always be cheaper. But the Am9080A, or any other fixed-instruction processor, can execute only one instruction set, so it is not really suitable for emulation of another machine.

Moreover, a fixed-instruction processor operates only on words of a single length, usually eight bits. An Am2900 design, on the other hand, can be constructed for any word length which is a multiple of four bits.

Many applications require specialized operations to be performed at relatively high speed. Such functions as multiply and divide and special graphic control operations, can be done in microcode 10–100 times faster than in fixed-instruction MOS processors.

MICROPROGRAMMED ARCHITECTURE

Most small processors today are being designed using a technique called microprogramming. In microprogrammed systems, a large portion of the system's control is performed by a read only memory (usually PROM) rather than large arrays of gates and flip-flops. This technique frequently reduces the package count in the controller and provides a highly ordered structure in the controller, not present when random logic is used. Moreover, microprogramming makes changes in the machines' instruction set very simple to perform – reducing the post-production engineering costs for the system substantially.

The Am2900 Family of Bipolar LSI devices has been designed for use in microprogrammed systems. Each device performs a basic system function and is driven by a set of control lines from a microinstruction.

Figure 3 illustrates a typical system architecture. There are two "sides" to the system. At the left is the control circuitry and on the right is the data manipulation circuitry. The block labeled "2901 array" consists of the ALU, scratchpad registers, data steering logic (all internal to the Am2901's), plus left/right shift control and carry lookahead circuit. Data is processed by moving it from main memory (not shown) into the 2901 registers, performing the required operations on it and returning the result to main memory. Memory addresses may also be generated in the 2901's and sent out to the memory address register (MAR). The four status bits from the 2901's ALU are captured in the status register after each operation.

The logic on the left side is the control section of the computer. This is where the Am2909 or Am2911 is used. The entire system is controlled by a memory, usually PROM, which contains long words called microinstructions. Each microinstruction contains bits to control each of the data manipulation elements in the system. There are, for example, nine bits for the 2901 instruction lines, eight bits for the A and B register addresses, two or three bits to control the shifting multiplexers at the ends of the 2901 array (Figure 19 or 2901 data sheet), and bits to control the register enables on the MAR, instruction register, and various bus transceivers. When the bits in a microinstruction are applied to all the data elements and everything is clocked, then one small operation (such as a data transfer or a register-to-register add) will occur.

A "machine instruction" (such as a minicomputer instruction or a 9080A instruction) is performed by executing several microinstructions in sequence. Each microinstruction therefore contains not only bits to control the data hardware, but also bits to define the location in PROM of the next microinstruction to be executed. The fields are labeled in Figure 3 as I, CC, and BA. The I field controls the sequencer. It indicates where the next address is located – the μPC, the stack, or the direct inputs – and whether the stack is to be pushed or popped.

The CC field contains bits indicating the conditions under which the I field applies. These are compared with the condition codes in the status register and may cause modification to the I field. The comparing and modification occurs in the block labeled "control logic". Frequently this is just a PROM. The BA field is a branch address or the address of a subroutine.

PIPELINING

The address for the microinstructions is generated by the sequencer, starting from a clock edge. The address goes from the sequencer to the ROM and, an access time later, the microinstruction is at the ROM outputs.

A pipeline register is a register placed on the output of the microprogram memory to essentially split the system in two. The pipeline register contains the microinstruction currently being executed ①. (Refer to the circled numbers in Figure 3.) The data manipulation control bits go out to the system elements and a portion of the microinstruction is returned to the sequencer ② to determine the address of the next microinstruction to be executed. That address ③ is sent to the ROM and the next microinstruction ④ sits at the input of the pipeline register. So while the 2901's are executing one instruction, the next instruction is being fetched from ROM. Note that there is no sequencial logic in the sequencer between the select lines and the output. This is important because the loop ① to ② to ③ to ④ must occur during a single clock cycle. During the same time, the loop from ① to ⑤ must occur in the 2901's. These two paths are roughly the same (around 200ns worst case for a 16-bit system). The presence of the pipeline register allows the microinstruction fetch to occur in parallel with the data operation rather than serially, allowing the clock frequency to be doubled.

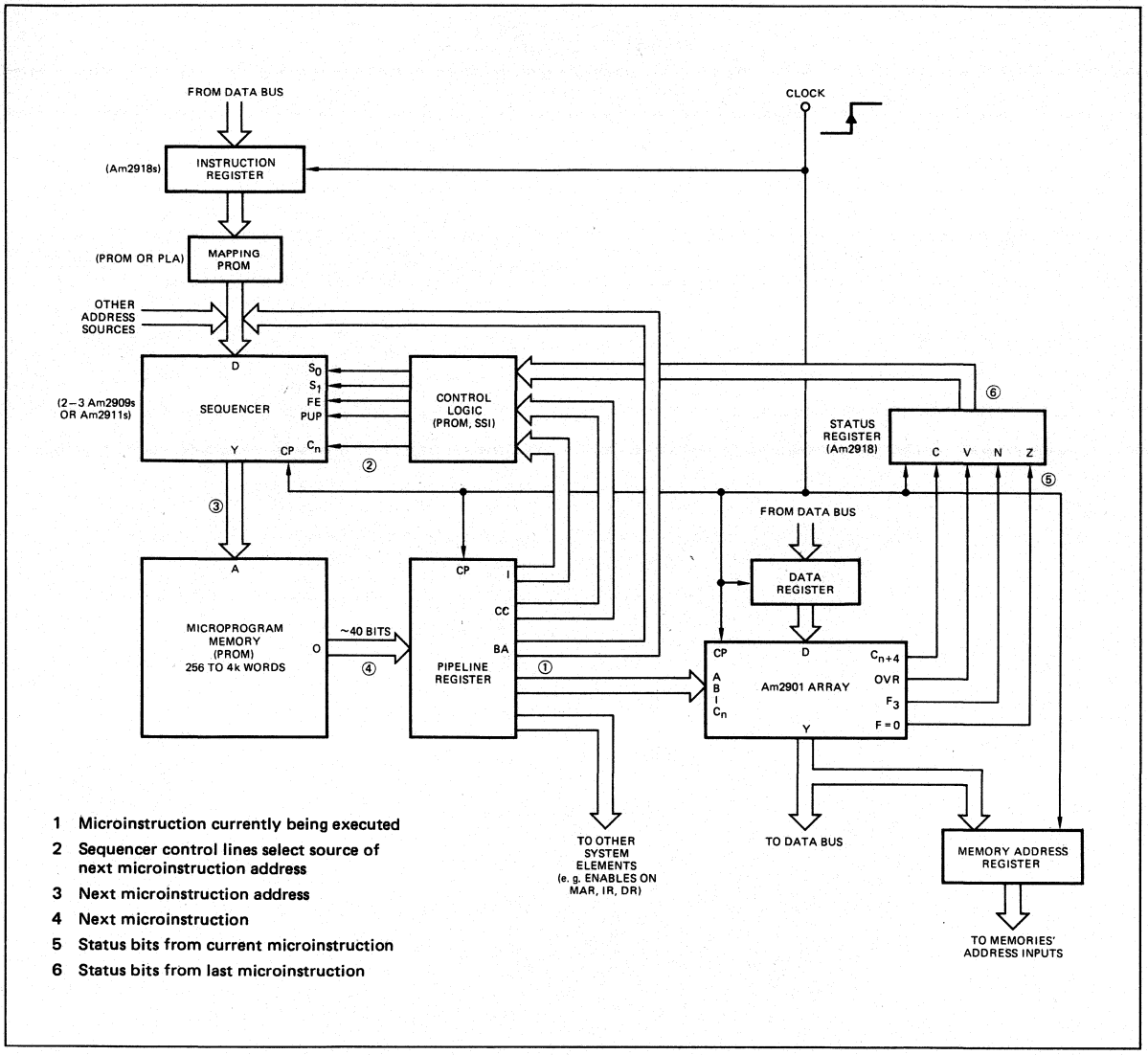


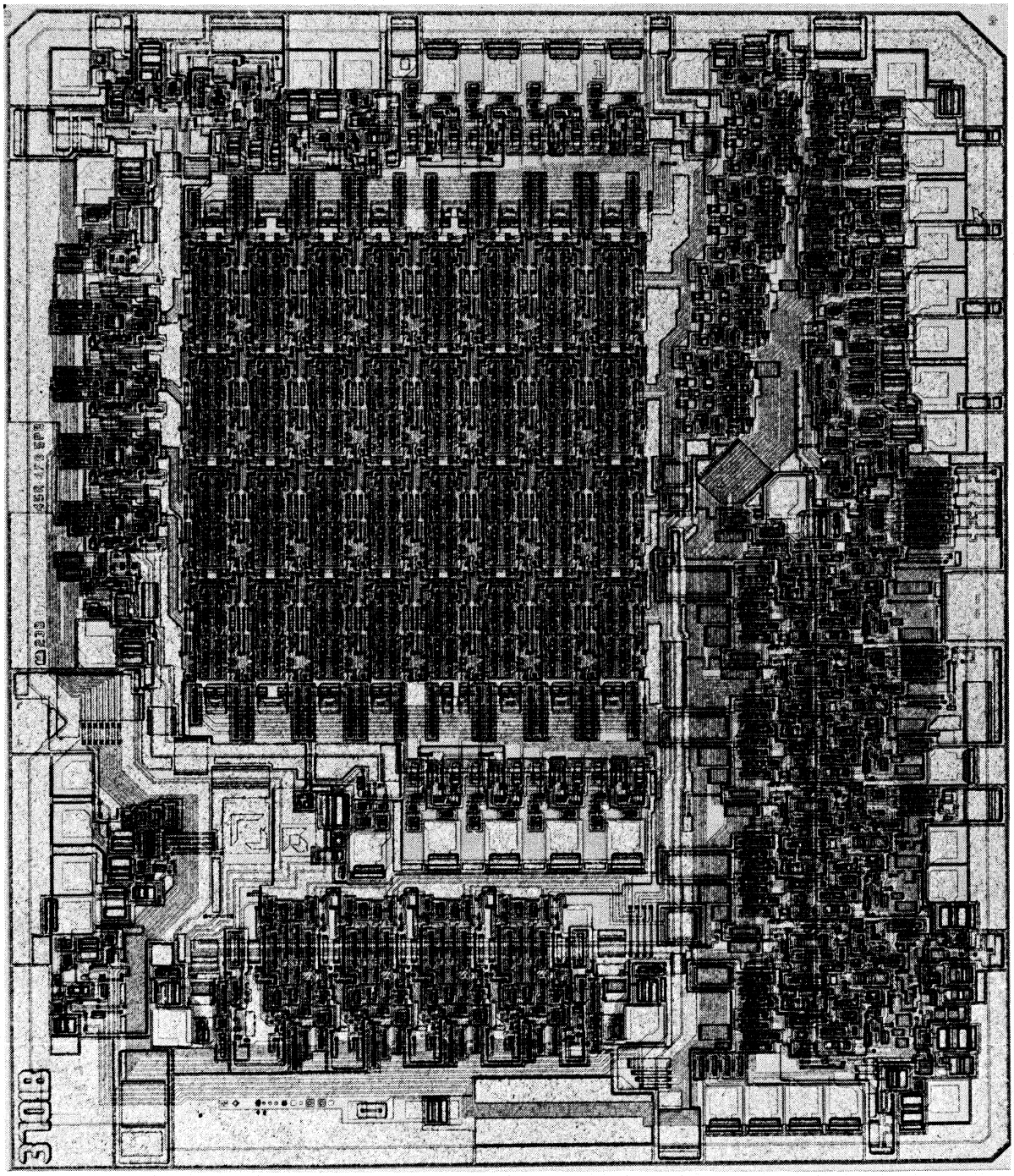
Figure 3.

The system shown in Figure 3 works as follows. A sequence of microinstructions in the PROM is executed to fetch an instruction from main memory. This requires that the program counter, often in a 2901 working register, be sent to the memory address register and incremented. The data returned from memory is loaded into the instruction register. The contents of the instruction register is passed through a PROM or PLA to generate the address of the first microinstruction which must be executed to perform the required function. A branch to this address occurs through the sequencer. Several microinstructions may be executed to fetch data from memory, perform ALU operations, test for overflow, and so forth. Then a branch will be made back to the instruction fetch cycle. At this point, there may be branches to other sections of microcode. For example, the machine might test for an interrupt here and obtain an interrupt service routine address from another mapping ROM rather than start on the next machine instruction. There are obviously many possibilities. Throughout this data book, in application notes, and within data sheets, some suggested techniques will be found.

Additional application notes are in preparation and are planned for publication during 1976. Advanced Micro Devices' Applications' staff is available to answer questions and provide technical assistance as well. They may be reached by calling (408) 732-2400, or, outside California (800) 538-7904. Ask for Am2900 Family Applications.

Am2901

Photomicrograph



Am2901

Four-Bit Bipolar Microprocessor Slice

DISTINCTIVE CHARACTERISTICS

- Two-address architecture –
  Independent simultaneous access to two working registers saves machine cycles.
- Eight-function ALU –
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- Flexible data source selection –
  ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.
- Left/right shift independent of ALU –
  Add and shift operations take only one cycle.
- Four status flags –
  Carry, overflow, zero, and negative.
- Expandable –
  Connect any number of Am2901's together for longer word lengths.
- Microprogrammable –
  Three groups of three bits each for source operand, ALU function, and destination control.

GENERAL DESCRIPTION

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the Am2901 will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

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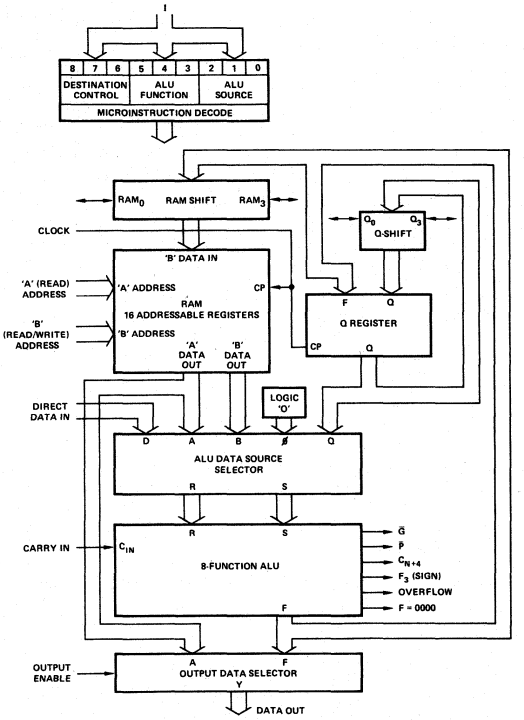
MICROPROCESSOR SLICE BLOCK DIAGRAM



ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The Am2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the Am2902 ('182). A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Figure 4.

The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Figure 4 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Figure 4.

The clock input to the Am2901 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

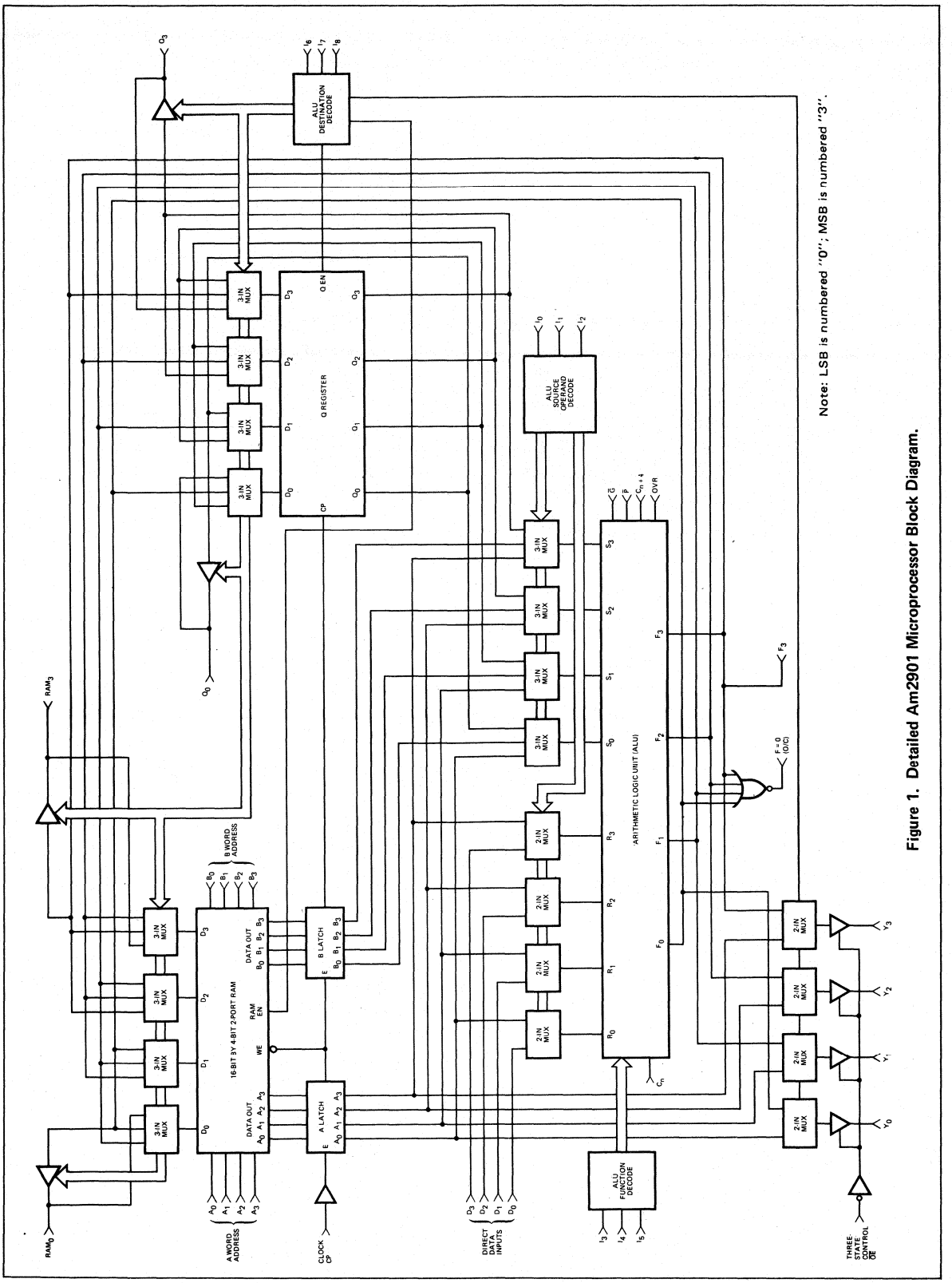


Figure 1. Detailed Am2901 Microprocessor Block Diagram.

MICRO CODE				ALU SOURCE OPERANDS	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	O	Q
L	H	H	3	O	B
H	L	L	4	O	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	O

Figure 2. ALU Source Operand Control.

MICRO CODE				ALU Function	Symbol
I_5	I_4	I_3	Octal Code		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S − R
L	H	L	2	R Minus S	R − S
L	H	H	3	R OR S	R ∨ S
H	L	L	4	R AND S	R ∧ S
H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
H	H	L	6	R EX-OR S	R ∀ S
H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control.

MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

X= Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
Up is toward MSB, Down is toward LSB.

Figure 4. ALU Destination Control.

OCTAL I_{210} OCTAL / I_{543} ALU Source / ALU Function	0	1	2	3	4	5	6	7
	A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0 C_n = L R Plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
0 C_n = H R Plus S	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1 C_n = L S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
1 C_n = H S Minus R	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2 C_n = L R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
2 C_n = H R Minus S	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3 R OR S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
4 R AND S	A∧Q	A∧B	0	0	0	D∧A	D∧Q	0
5 $\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6 R EX-OR S	A∀Q	A∀B	Q	B	A	D∀A	D∀Q	D
7 R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ∀ = EX-OR

Figure 5. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Figure 5 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 6 defines the various logic operations that the Am2901 can perform and Figure 7 shows the arithmetic functions of the device. Both carry-in LOW (C_n = 0) and carry-in HIGH (C_n = 1) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	A∧Q
4 1		A∧B
4 5		D∧A
4 6		D∧Q
3 0	OR	A∨Q
3 1		A∨B
3 5		D∨A
3 6		D∨Q
6 0	EX-OR	A∀Q
6 1		A∀B
6 5		D∀A
6 6		D∀Q
7 0	EX-NOR	$\overline{A \forall Q}$
7 1		$\overline{A \forall B}$
7 5		$\overline{D \forall A}$
7 6		$\overline{D \forall Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$∧Q
5 1		$\overline{A}$∧B
5 5		$\overline{D}$∧A
5 6		$\overline{D}$∧Q

Figure 6. ALU Logic Mode Functions. (C_n Irrelevant)

Octal	C_n = 0 (Low)		C_n = 1 (High)	
I_{543}, I_{210}	Group	Function	Group	Function
0 0	ADD	A+Q	ADD plus one	A+Q+1
0 1		A+B		A+B+1
0 5		D+A		D+A+1
0 6		D+Q		D+Q+1
0 2	PASS	Q	Increment	Q+1
0 3		B		B+1
0 4		A		A+1
0 7		D		D+1
1 2	Decrement	Q–1	PASS	Q
1 3		B–1		B
1 4		A–1		A
2 7		D–1		D
2 2	1's Comp.	–Q–1	2's Comp. (Negate)	–Q
2 3		–B–1		–B
2 4		–A–1		–A
1 7		–D–1		–D
1 0	Subtract (1's Comp)	Q–A–1	Subtract (2's Comp)	Q–A
1 1		B–A–1		B–A
1 5		A–D–1		A–D
1 6		Q–D–1		Q–D
2 0		A–Q–1		A–Q
2 1		A–B–1		A–B
2 5		D–A–1		D–A
2 6		D–Q–1		D–Q

Figure 7. ALU Arithmetic Mode Functions.

LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the Am2901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 2.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$
$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$
$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$
$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$$

$$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$

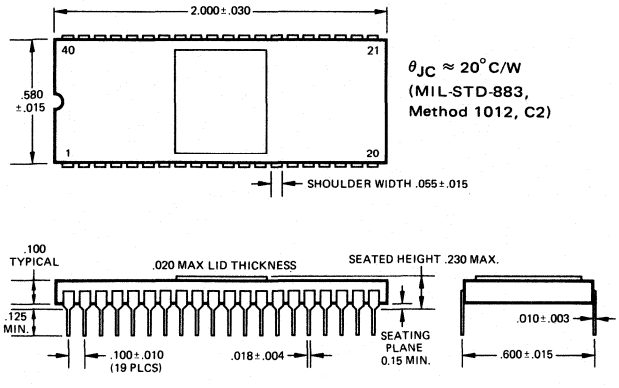
I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R ∀ S	← Same as $\overline{R \forall S}$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0 (G_0 + \overline{C_n})}$	See note

Note: $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$ + = OR

Figure 8.

PACKAGE OUTLINE

40-Pin Ceramic (Side Brazed)



42-Pin Flat Package

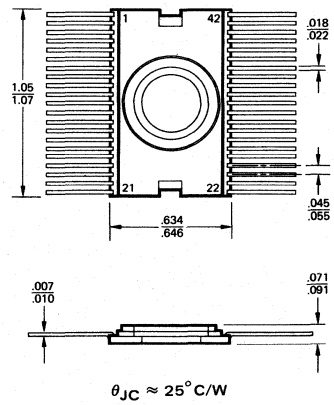
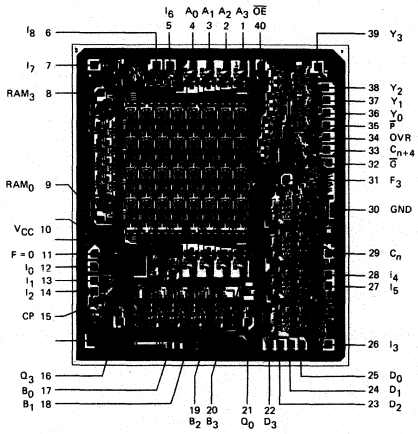


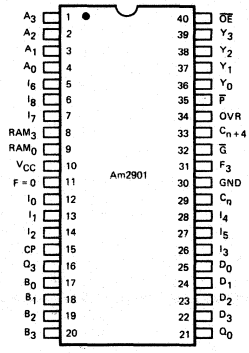
Figure 9.

METALLIZATION AND PAD LAYOUT



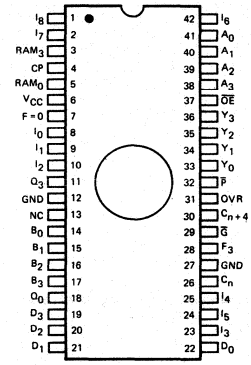
DIE SIZE 0.167" x 0.198"

CONNECTION DIAGRAM
Top View
DIP



Note: Pin 1 is marked for orientation.

FLAT PACK CONNECTIONS
Top View



Note: Both grounds (pins 12 and 27) must be connected.

Figure 10.

PIN DEFINITIONS

A_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8} The nine instruction control lines to the Am2901, used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3 RAM_3 A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the Am2901. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM_0 Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-3} Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the Am2901. D_0 is the LSB.

Y_{0-3} The four data outputs of the Am2901. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{P}$, $\overline{G}$ The carry generate and propagate outputs of the Am2901's ALU. These signals are used with the Am2902 for carry-lookahead. See Figure 8 for the logic equations.

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit. See Figure 8 for logic equation.

F = 0 This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

C_n The carry-in to the Am2901's ALU.

C_{n+4} The carry-out of the Am2901's ALU. See Figure 8 for equations.

CP The clock to the Am2901. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which comprises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +6.3 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

P/N	Ambient Temperature	V_{CC}
Am2901PC, DC	0°C to +70°C	4.75 V to 5.25 V
Am2901DM, FM	−55°C to +125°C	4.50 V to 5.50 V

STANDARD SCREENING

(Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Level Am2901PC, DC	Level Am2901DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C 24-hour 150°C	100%	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B 10,000 G	100% *	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/cm^3	100% *	100%
Gross Leak	1014	C2 Fluorocarbon	100% *	100%
Electrical Test Subgroups 1 and 7	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 7
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 7

*Not applicable for Am2901PC

ADDITIONAL SCREENING FOR CLASS B PARTS

Step	MIL-STD-883 Method	Conditions	Level Am2901DMB, FMB
Burn-In	1015	D 125°C 160 hours min.	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2901PC
Hermetic DIP	0°C to +70°C	AM2901DC
Hermetic DIP	−55°C to +125°C	AM2901DM
Hermetic Flat Pack	−55°C to +125°C	AM2901FM
Dice	0°C to +70°C	AM2901XC

GROUP A SUBGROUPS

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum Rated Temeperature
11	Switching	Minimum Rated Temperature

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

(Group A, Subgroups 1, 2 and 3)

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_0, Y_1, Y_2, Y_3	2.4			Volts
			I_{OH} = −1.0mA, C_{n+4}	2.4			
			I_{OH} = −800μA, OVR, $\overline{P}$	2.4			
			I_{OH} = −600μA, F_3	2.4			
			I_{OH} = −600μA $RAM_{0,3}$, $Q_{0,3}$	2.4			
			I_{OH} = −1.6mA, $\overline{G}$	2.4			
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}				250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA $Y_0, Y_1, Y_2, Y_3, \overline{G}$			0.5	Volts
			I_{OL} = 10mA, C_{n+4}, F=0			0.5	
			I_{OL} = 8.0mA, OVR, $\overline{P}$			0.5	
			I_{OL} = 6.0mA, F_3 $RAM_{0,3}$, $Q_{0,3}$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	Military			0.7	Volts
			Commercial			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX. V_{IN} = 0.5V	Clock, $\overline{OE}$			−0.36	mA
			A_0, A_1, A_2, A_3			−0.36	
			B_0, B_1, B_2, B_3			−0.36	
			D_0, D_1, D_2, D_3			−0.72	
			I_0, I_1, I_2, I_6, I_8			−0.36	
			I_3, I_4, I_5, I_7			−0.72	
			$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			−0.8	
			C_n			−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX. V_{IN} = 2.7V	Clock, $\overline{OE}$			20	μA
			A_0, A_1, A_2, A_3			20	
			B_0, B_1, B_2, B_3			20	
			D_0, D_1, D_2, D_3			40	
			I_0, I_1, I_2, I_6, I_8			20	
			I_3, I_4, I_5, I_7			40	
			$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			100	
			C_n			200	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.	Y_0, Y_1, Y_2, Y_3 V_O = 2.4V			50	μA
			Y_0, Y_1, Y_2, Y_3 V_O = 0.5V			−50	
			$RAM_{0,3}$, $Q_{0,3}$ V_O = 2.4V (Note 4)			100	
			$RAM_{0,3}$, $Q_{0,3}$ V_O = 0.5V (Note 4)			−800	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75V V_O = 0.5V	$Y_0, Y_1, Y_2, Y_3, \overline{G}$	−15		−40	mA
			C_{n+4}	−15		−40	
			OVR, $\overline{P}$	−15		−40	
			F_3	−15		−40	
			$RAM_{0,3}$, $Q_{0,3}$	−15		−40	
I_{CC}	Power Supply Current	V_{CC} = MAX.	Military		185	280	mA
			Commercial		185	280	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.

GUARANTEED OPERATING CONDITIONS OVER TEMPERATURE AND VOLTAGE

Tables I, II, and III below define the timing requirements of the Am2901 in a system. The Am2901 is guaranteed to function correctly over the operating range when used within the delay and set-up time constraints of these tables for the appropriate device type. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

The performance of the Am2901 within the limits of these tables is guaranteed by the testing defined as "Group A, Subgroup 9" Electrical Testing. For a copy of the tests and limits used for subgroup 9, contact Advanced Micro Devices' Product Marketing.

TABLE I

CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	Am2901DC, PC	Am2901DM, FM
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	105ns	120ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle)	9.5MHz	8.3MHz
Minimum Clock LOW Time	30ns	30ns
Minimum Clock HIGH Time	30ns	30ns
Minimum Clock Period	105ns	120ns

TABLE II

MAXIMUM COMBINATIONAL PROPAGATION DELAYS (all in ns, $C_L \leq 15pF$)

From Input \ To Output	Am2901DC, PC (0°C to +70°C; 5V ±5%)								Am2901DM, FM (−55°C to +125°C; 5V ±10%)							
	Y	F_3	C_{n+4}	$\overline{G}, \overline{P}$	F=0 R_L= 470	OVR	Shift Outputs		Y	F_3	C_{n+4}	$\overline{G}, \overline{P}$	F=0 R_L= 470	OVR	Shift Outputs	
							RAM_0 RAM_3	Q_0 Q_3							RAM_0 RAM_3	Q_0 Q_3
A, B	110	85	80	80	110	75	110	–	120	95	90	90	120	85	120	–
D (arithmetic mode)	100	70	70	70	100	60	95	–	110	80	75	75	110	65	105	–
D (I = X37) (Note 5)	60	50	–	–	60	–	60	–	65	55	–	–	65	–	65	–
C_n	55	35	30	–	50	40	55	–	60	40	30	–	55	45	60	–
I_{012}	85	65	65	65	80	65	80	–	90	70	70	70	85	70	85	–
I_{345}	70	55	60	60	70	60	65	–	75	60	65	65	75	65	70	–
I_{678}	55	–	–	–	–	–	45	45	60	–	–	–	–	–	50	50
$\overline{OE}$ Enable/Disable	40/25	–	–	–	–	–	–	–	40/25	–	–	–	–	–	–	–
A bypassing ALU (I = 2xx)	60	–	–	–	–	–	–	–	65	–	–	–	–	–	–	–
Clock ⌐ (Note 6)	115	85	100	100	110	95	105	60	125	95	110	110	120	105	115	65

SET-UP AND HOLD TIMES (all in ns) (Note 1)

TABLE III

From Input	Notes	Am2901DC, PC (0°C to +70°C, 5V ±5%)		Am2901DM, FM (−55°C to +125°C, 5V ±10%)	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
A, B Source	2, 4 3, 5	105 $t_{pw}L$ + 30	0	120 $t_{pw}L$ + 30	0
B Dest.	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ +15	0
D (arithmetic mode)		100	0	110	0
D (I = X37) (Note 5)		60	0	65	0
C_n		55	0	60	0
I_{012}		85	0	90	0
I_{345}		70	0	75	0
I_{678}	4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
$RAM_{0, 3}$, $Q_{0, 3}$		30	0	30	0

Notes: 1. See Figure 11 and 12.
2. If the B address is used as a source operand, allow for the "A, B source" set-up time; if it is used only for the destination address, use the "B dest." set-up time.
3. Where two numbers are shown, both must be met.
4. "$t_{pw}L$" is the clock LOW time.
5. DV0 is the fastest way to load the RAM from the D inputs. This function is obtained with I = 337.
6. Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

SET-UP AND HOLD TIMES (minimum cycles from each input)

Set-up and hold times are defined relative to the clock LOW-to-HIGH edge. Inputs must be steady at all times from the set-up time prior to the clock until the hold time after the clock. The set-up times allow sufficient time to perform the correct operation on the correct data so that the correct ALU data can be written into one of the registers.

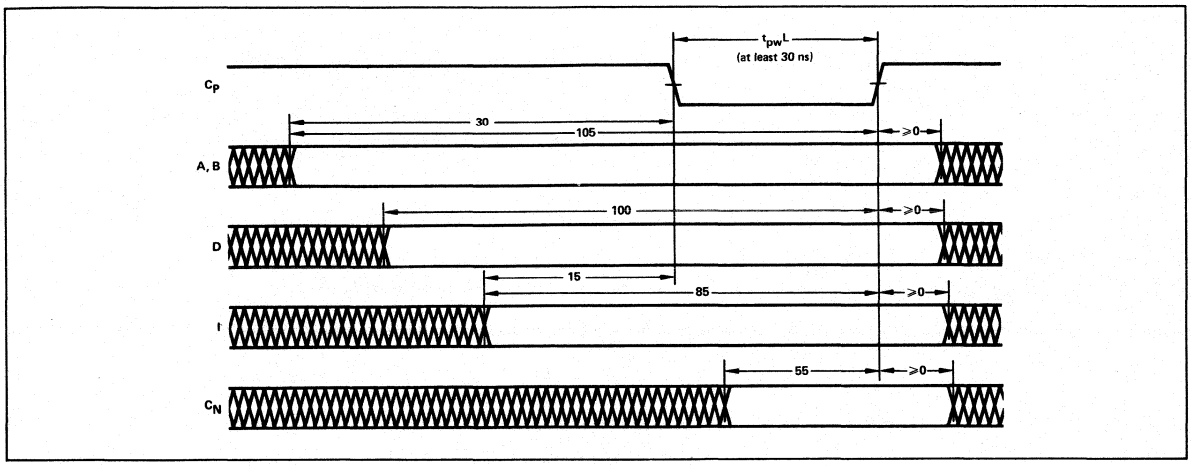
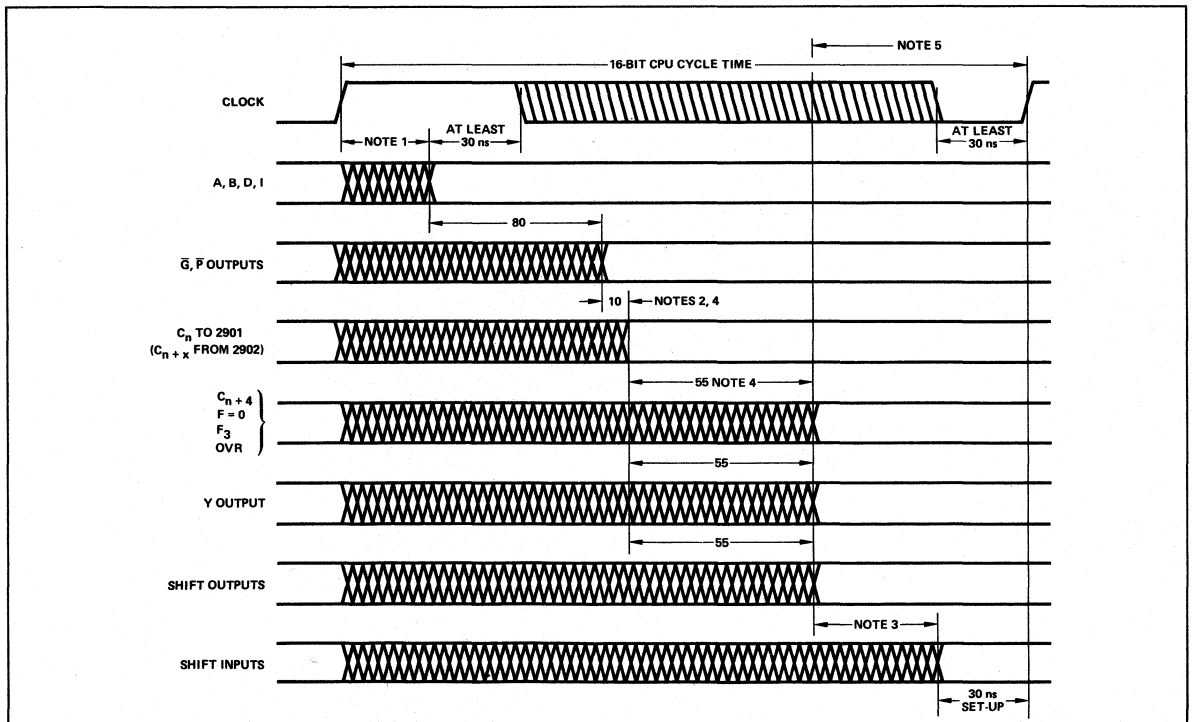


Figure 11. Minimum Cycle Times from Inputs. Numbers Shown are Minimum Data Stable Times for Am2901DC, in ns. See Table III for Detailed Information.



Notes:
1. This delay is the max. t_{pd} of the register containing A, B, D, and I. For the Am2918, use 13ns.
2. 10ns for look-ahead carry. For ripple carry over 16 bits use 2 x ($C_n \rightarrow C_{n+4}$), or 60ns.
3. This is the delay associated with the multiplexer between the shift outputs and shift inputs on the Am2901s. See Figure 19.
4. Not applicable for logic operations.
5. Clock rising edge may occur here if add and shift do not occur on same cycle.

Figure 12. Switching Waveforms for 16-Bit System Assuming A, B, D and I are all Driven from Registers with the same Propagation Delay, Clocked by the Am2901 Clock.

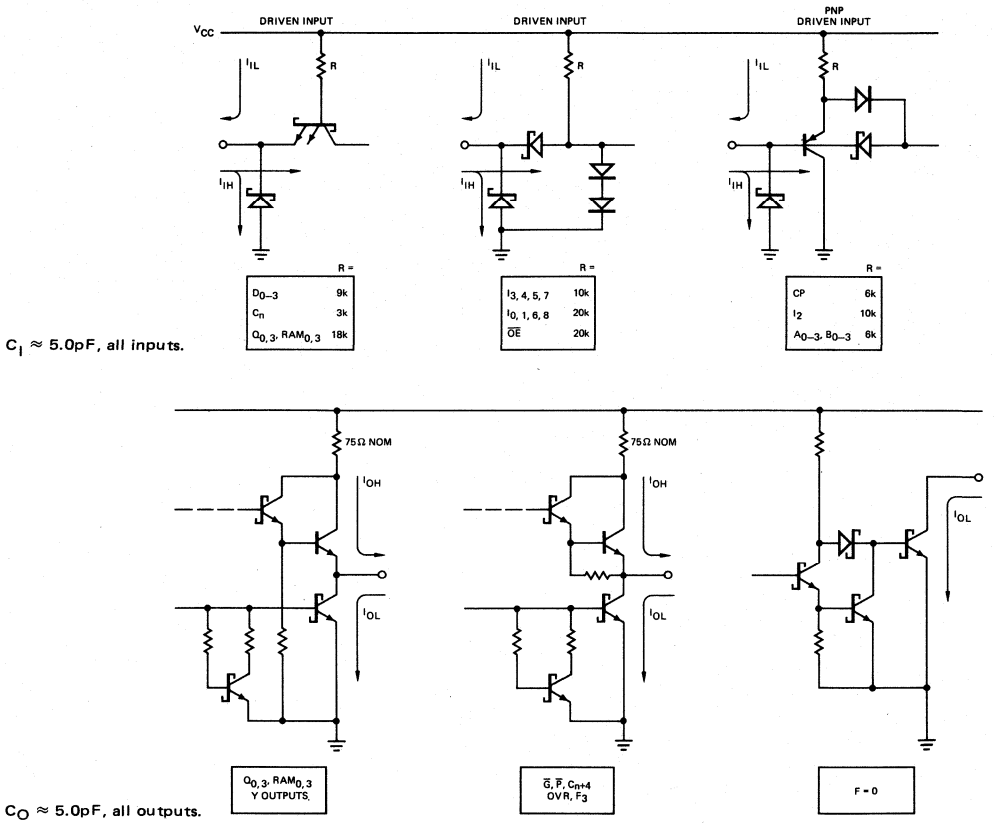


Figure 13. Am2901 Input/Output Current Interface Conditions.

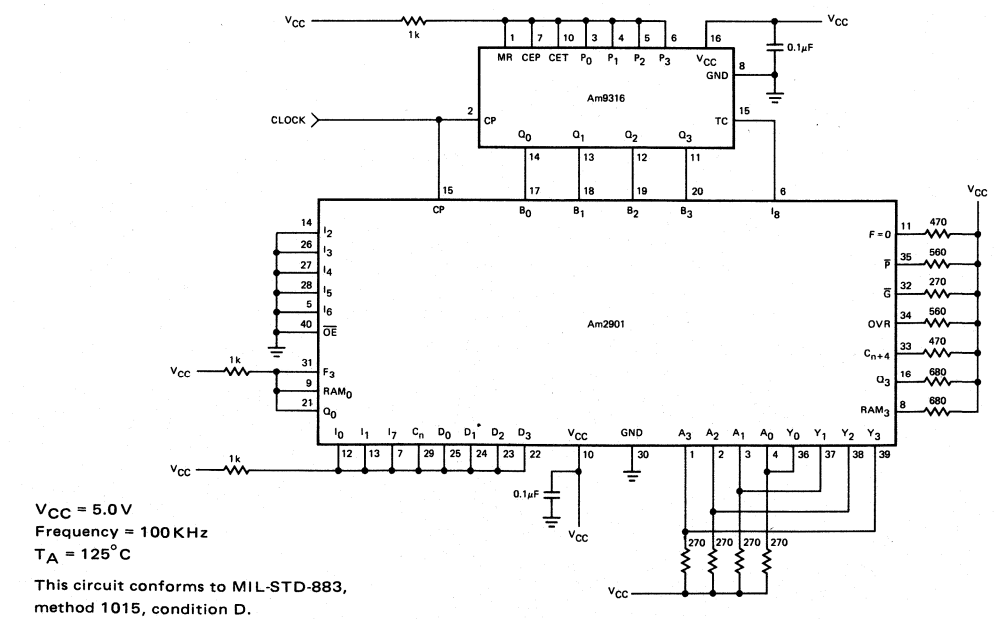


Figure 14. Am2901 Burn-In Circuit.

USING THE Am2901

BASIC SYSTEM ARCHITECTURE

The Am2901 is designed to be used in microprogrammed systems. Figure 15 illustrates such an architecture. The nine instruction lines, the A and B addresses, and the D data inputs normally will all come from registers clocked at the same time as the Am2901. The register inputs come from a ROM or PROM – the "microprogram store". This memory contains sequences of microinstructions, typically 28 to 40 bits wide, which apply the proper control signals to the Am2901's and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2909 microprogram sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2909 is controlled by some of the bits coming from the microprogram store. Essentially these bits are the "next instruction" control.

Note that with the microprogram register in-between the microprogram memory store and the Am2901's, an instruction accessed on one cycle is executed on the next cycle. As one instruction is executed, the next instruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am2901's occurs in parallel with the access time of the microprogram store. Without the "pipeline register", these two functions must occur serially.

EXPANSION OF THE Am2901

The Am2901 is a four-bit CPU slice. Any number of Am2901's can be interconnected to form CPU's of 12, 16, 24, 36 or more bits, in four-bit increments. Figure 16 illustrates the interconnection of three Am2901's to form a 12-bit CPU, using ripple carry. Figure 17 illustrates a 16-bit CPU using carry lookahead, and Figure 18 is the general carry lookahead scheme for long words.

With the exception of the carry interconnection, all expansion schemes are the same. Refer to Figure 14. The Q_3 and RAM_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the Q_0 and RAM_0 pins of the adjacent more significant device. These connections allow the Q-registers of all Am2901's to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to three-state multiplexers which can be controlled by the microcode to select the appropriate input signals to the shift inputs. (See Figure 19)

The open collector F = 0 outputs of all the Am2901's are connected together and to a pull-up resistor. This line will go HIGH if and only if the output of the ALU contains all zeroes. Most systems will use this line as the Z (zero) bit of the processor status word.

The overflow and F_3 pins are generally used only at the most significant end of the array, and are meaningful only when two's complement signed arithmetic is used. The overflow pin is the Exclusive-OR of the carry-in and carry-out of the sign bit (MSB). It will go HIGH when the result of an arithmetic

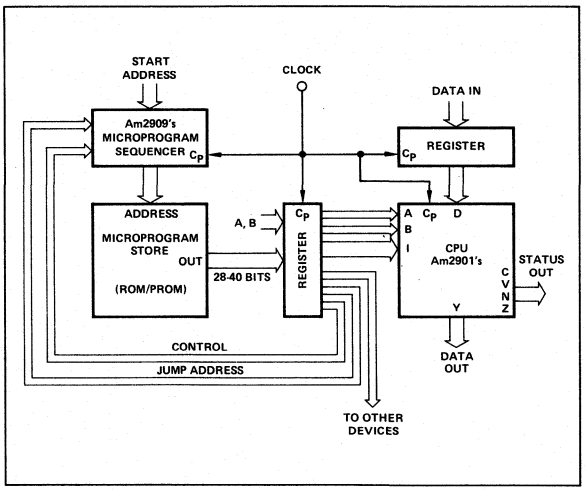


Figure15. Microprogrammed Architecture Around Am2901's.

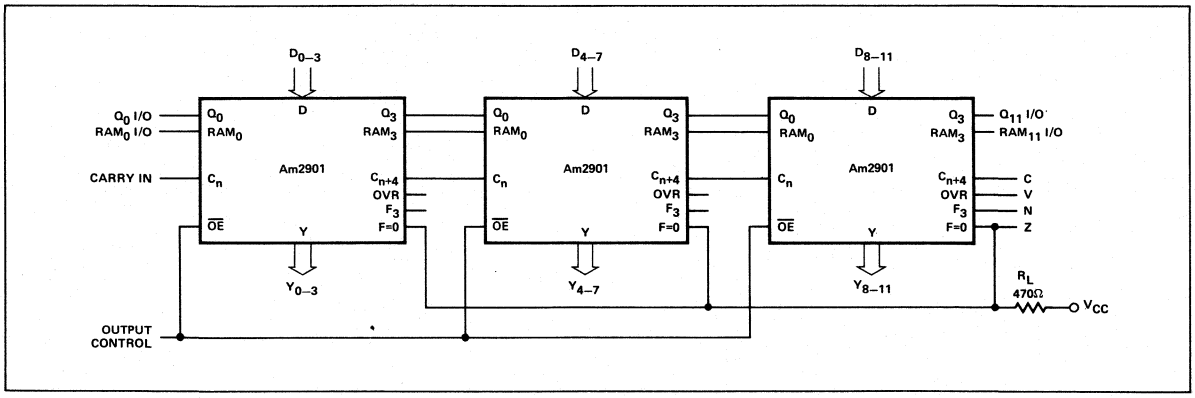


Figure 16. Three Am2901's used to Construct 12-Bit CPU with Ripple Carry. Corresponding A, B, and I Pins on all Devices are Connected Together.

operation is a number requiring more bits than are available, causing the sign bit to be erroneous. This is the overflow (V) bit of the processor status word. The F_3 pin is the MSB of the ALU output. It is the sign of the result in two's complement notation, and should be used as the Negative (N) bit of the processor status word.

The carry-out from the most significant Am2901 (C_{n+4} pin) is the carry-out from the array, and is used as the carry (C) bit of the processor status word.

Carry interconnections between devices may use either ripple carry or carry lookahead. For ripple carry, the carry-out (C_{n+4}) of each device is connected to the carry-in (C_n) of the next more significant device. Carry lookahead uses the Am2902 lookahead carry generator. The scheme is identical to that used with the 74181/74182. Users unfamiliar with this technique should refer to AMD's application note on Arithmetic Logic Units. Figures 17 and 18 illustrate single and multiple level lookahead.

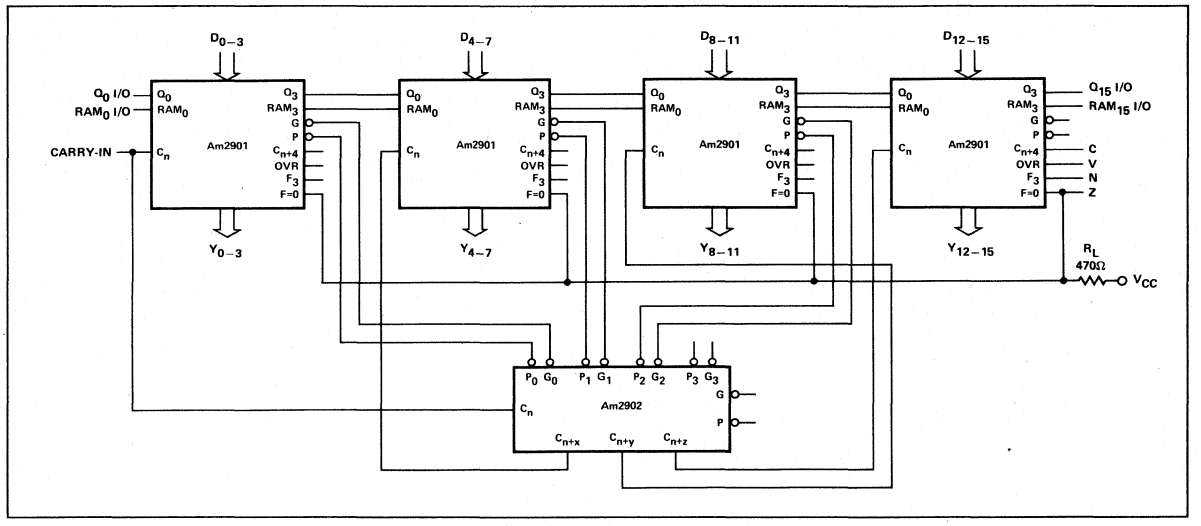


Figure 17. Four Am2901's in a 16-Bit CPU using the Am2902 for Carry Lookahead.

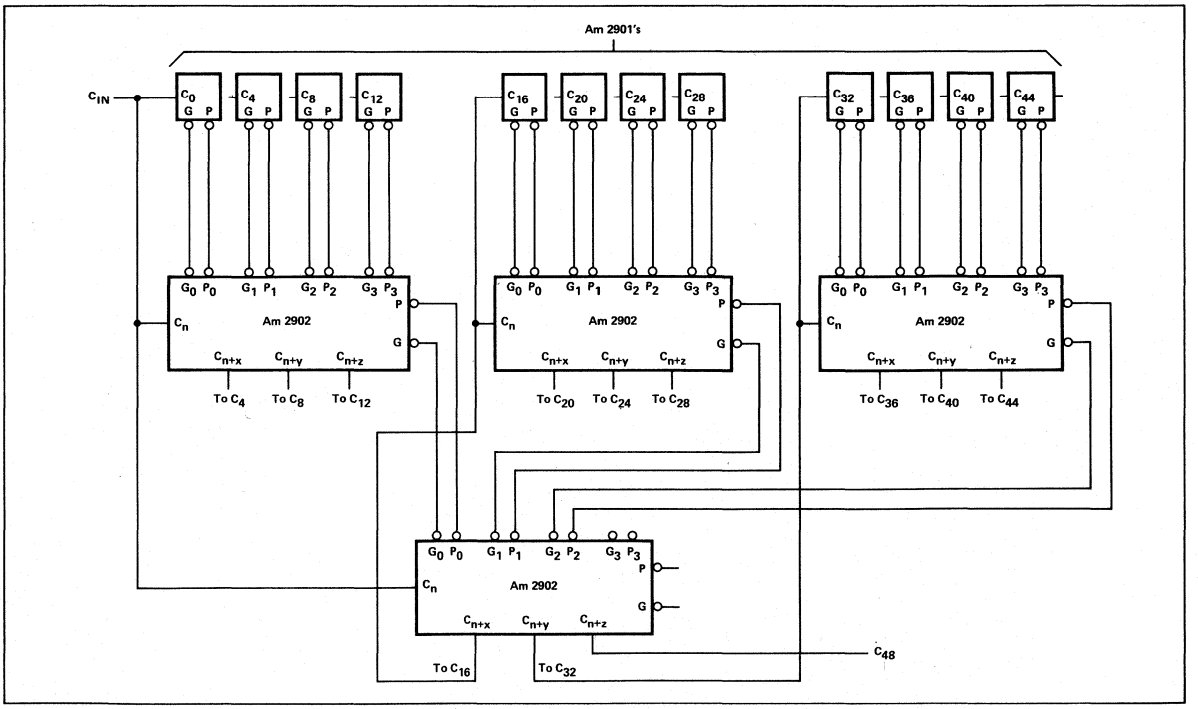


Figure 18. Carry Lookahead Scheme for 48-Bit CPU using 12 Am2901's. The Carry-Out Flag (C_{48}) Should be Taken from the Lower Am2902 Rather than the Right-Most Am2901 for Higher Speed.

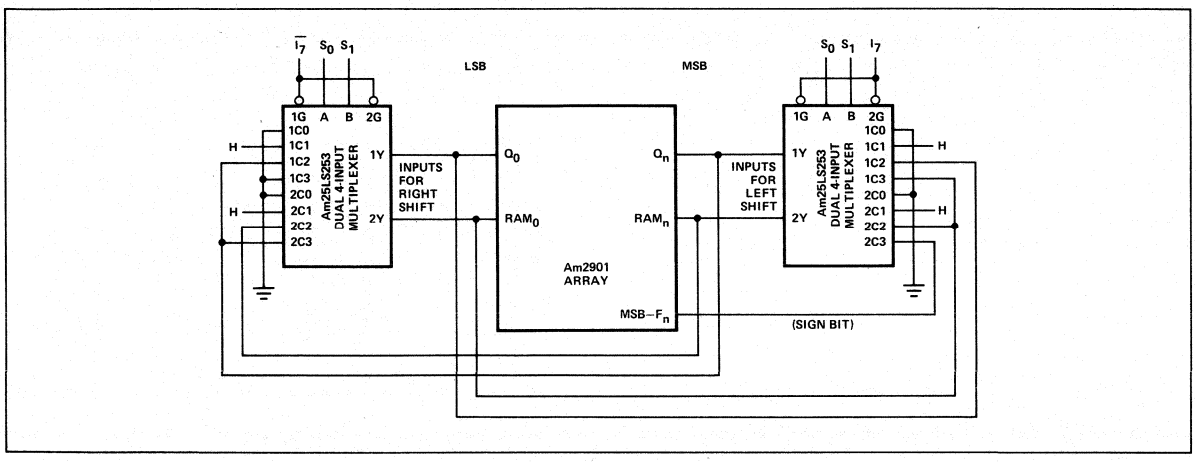


Figure 19. Three-State Multiplexers Used on Shift I/O Lines.

SHIFT I/O LINES AT THE END OF THE ARRAY

The Q-register and RAM left/right shift data transfers occur between devices over bidirectional lines. At the ends of the array, three-state multiplexers are used to select what the new inputs to the registers should be during shifting. Figure 19 shows two Am25LS253 dual four-input multiplexers connected to provide four shift modes. Instruction bit I_7 (from the Am2901) is used to select whether the left-shift multiplexer or the right-shift multiplexer is active. The four shift modes in this example are:

Zero A LOW is shifted into the MSB of the RAM on a down shift. If the Q-register is also shifted, then a LOW is deposited in the Q-register MSB. If the RAM or both registers are shifted up, LOWs are placed in the LSBs.

One Same as zero, but a HIGH level is deposited in the LSB or MSB.

Rotate A single precision rotate. The RAM MSB shifts into the LSB on a right shift and the LSB shifts into the MSB on a left shift. The Q-register, if shifted, will rotate in the same manner.

Arithmetic A double-length Arithmetic Shift if Q is also shifted. On an up shift a zero is loaded into the Q-register LSB and the Q-register MSB is loaded into the RAM LSB. On a down shift, the RAM LSB is loaded into the Q-register MSB and the ALU output MSB (F_n, the sign bit) is loaded into the RAM MSB. (This same bit will also be in the next less significant RAM bit.)

Code			Source of New Data				Shift	Type
I_7	S_1	S_0	Q_0	Q_n	RAM_0	RAM_n		
H	L	L	0	Q_{n-1}	0	F_{n-1}	Up	Zero
H	L	H	1	Q_{n-1}	1	F_{n-1}	(Right)	One
H	H	L	Q_n	Q_{n-1}	F_n	F_{n-1}		Rotate
H	H	H	0	Q_{n-1}	Q_n	F_{n-1}		Arithmetic
L	L	L	Q_1	0	F_1	0	Down	Zero
L	L	H	Q_1	1	F_1	1	(Left)	One
L	H	L	Q_1	Q_0	F_1	F_0		Rotate
L	H	H	Q_1	F_0	F_1	$RAM_n = RAM_{n-1} = F_n$		Arithmetic

HARDWARE MULTIPLICATION

Figure 20 illustrates the interconnections for a hardware multiplication using the Am2901. The system shown uses two devices for 8 x 8 multiplication, but the expansion to more bits is simple — the significant connections are at the LSB and MSB only.

The basic technique used is the "add and shift" algorithm. One clock cycle is required for each bit of the multiplier. On each cycle, the LSB of the multiplier is examined; if it is a "1", then the multiplicand is added to the partial product to generate a new partial product. The partial product is then shifted one place toward the LSB, and the multiplier is also shifted one place toward the LSB. The old LSB of the multiplier is discarded. The cycle is then repeated on the new LSB of the multiplier available at Q_0.

The multiplier is in the Am2901 Q-register. The multiplicand is in one of the registers in the register stack, R_a. The product will be developed in another of the registers in the stack, R_b.

The A address inputs are used to address the multiplicand in R_a, and the B address inputs are used to address the partial product in R_b. On each cycle, R_a is conditionally added to R_b, depending on the LSB of Q as read from the Q_0 output, and both Q and the ALU output are shifted left one place. The instruction lines to the Am2901 on every cycle will be:

I_{876} = 4 (shift register stack input and Q register left)
I_{543} = 0 (Add)
I_{210} = 1 or 3 (select A, B or 0, B as ALU sources)

Figure 20 shows the connections for multiplication. The circled numbers refer to the paragraphs below.

1. The adjacent pins of the Q-register and RAM shifters are connected together so that the Q-registers of both (or all) Am2901's shift left or right as a unit. Similarly, the entire eight-bit (or more) ALU output can be shifted as a unit prior to storage in the register stack.

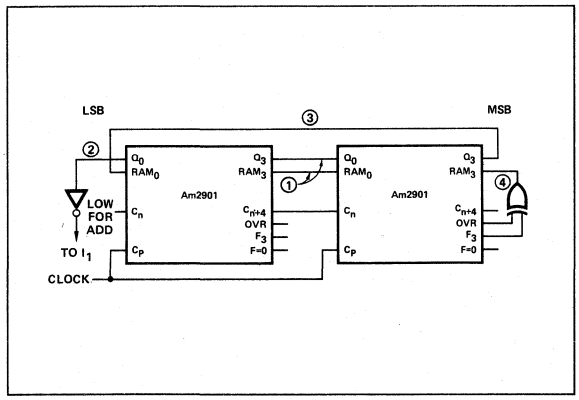


Figure 20. Interconnection for Dedicated Multiplication (8 by 8 Bit) (Corresponding A, B and I Connected Together).

2. The shift output at the LSB of the Q-register determines whether the ALU source operands will be A and B (add multiplicand to partial product) or 0 and B (add nothing to partial product. Instruction bit I_1 can select between A, B or 0, B as the source operands; it can be driven directly from the complement of the LSB of the multiplier.

3. As the new partial product appears at the input to the register stack, it is shifted left by the RAM shifter. The new LSB of the partial product, which is complete and will not be affected by future operations, is available on the RAM_0 pin. This signal is returned to the MSB of the Q-register. On each cycle then, the just-completed LSB of the product is deposited in the MSB of the Q-register; the Q-register fills with the least significant half of the product.

4. As the ALU output is shifted down on each cycle, the sign bit of the new partial product should be inserted in the RAM MSB shift input. The F_3 flag will be the correct sign of the partial product unless overflow has occurred. If overflow occurs during an addition or subtraction, the OVR flag will go HIGH and F_3 is not the sign of the result. The sign of the result must then be the complement of F_3. The correct sign bit to shift into the MSB of the partial product is therefore F3 ⊕ OVR; that is, F_3 if overflow has not occurred and $\overline{F_3}$ if overflow has occurred. On the last cycle, when the MSB of the multiplier is examined, a conditional subtraction rather than addition should be performed, because the sign bit of the multiplier carries negative rather than positive arithmetic weight

$$(Y = -Y_i 2^i + Y_{i-1} 2^{i-1} + \ldots + Y_0 2^0).$$

This scheme will produce a correct two's complement product for all multiplicands and multipliers in two's complement notation.

Figure 21 is a table showing the input states of the Am2901's for each step of a signed, two's complement multiplication.

Initial Register States

R

0	Multiplier
1	Multiplicand
2	X
3	X

Am2901 Microcode

Program 2's Comp. Multiply

Date 8/5/75 By J. S.

Final Register States

R

0	Multiplier
1	Multiplicand
2	LSH Product
3	MSH Product

S, F →	D	Description	Repeat	Pin States (Octal)										Jump	
				A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	To	If
O ∨ A	Q	Move Multiplier to Q	–	0	X	0	3	4	X	X	X	X	X		
O ∧ B	B	Clear R_3	–	X	3	2	4	3	X	X	X	X	X		
(O+B)/2 (A+B)/2	B	Cond. Add & Shift	n–1	1	3	4	0	1 or 3 $I_1 = Q_0 LO$	0	–	RAM_0	–	$F_3 \forall OVR$		
(B–O)/2 (B–A)/2	B	Cond. Subt. & Shift	–	1	3	4	1	1 or 3 $I_1 = Q_0 LO$	1	–	RAM_0	–	$F_3 \forall OVR$		
O ∨ Q	B	Move LSH Prod. to R_2	–	X	2	2	3	2	X	X	X	X	X		

X = Don't Care S = Source F = Function D = Destination

Figure 21.

EXAMPLES OF SOME OTHER OPERATIONS

1. Byte Swapping

Occasionally the two halves of a 16-bit word must be swapped. D_{0-7} is interchanged with D_{8-15}. The quickest way to perform this operation is to rotate the word in RAM, shifting two bits at a time. Only four shift cycles are required. The same register is selected on both the A and B ports; the two are added together with carry-in connected to carry-out, producing a right shift of one place; then the ALU is shifted right one more place prior to storage.

Byte Swap of R_0

$A = B = 0$ $I = 701$ $RAM_0 = RAM_{15}$ $C_{IN} = C_{OUT}$

Repeat 4 times

2. Instruction Fetch Cycle

Execution of a macroinstruction generally begins with an instruction fetch cycle. The current contents of the PC (in one of the registers) is the address of the macroinstruction to be fetched, and must be read out to the memory address register. Then the PC is incremented to point to the next macroinstruction. The macroinstruction obtained from memory is then loaded into the Am2909 microprogram sequencer to cause a jump to the microcode for executing the instruction.

The PC can be read out and incremented in one cycle by using the Am2901 destination code 2, and addressing the PC with both the A and B addresses. The current value of PC will appear on the Y outputs, and PC+1 will be returned to the register. If the PC is in register 15, then:

A = B = 15, I = 203, Carry-in = 1

The PC will be on the Y outputs via the RAM A-port. On the clock LOW-to-HIGH transition, the program counter is incremented and the value on the Y outputs is loaded into the memory address register. During the following cycle, the memory is read and, on the next clock LOW-to-HIGH transition the instruction from the memory is dropped into the Am2909 instruction register. The fetch operation requires only two microcycles.

Am2902

High-Speed Look-Ahead Carry Generator

Distinctive Characteristics

- Provides look-ahead carries across a group of four Am2901 microprocessor ALU's
- Capability of multi-level look-ahead for high-speed arithmetic operation over large word lengths
- Typical carry propagation delay of 6 ns
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

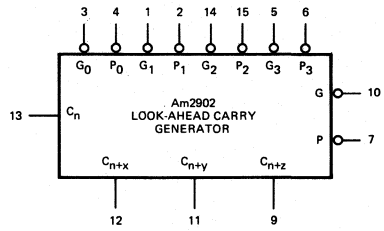
The Am2902 is a high-speed, look-ahead carry generator which accepts up to four pairs of carry propagate and carry generate signals and a carry input and provides anticipated carries across four groups of binary ALU's. The device also has carry propagate and carry generate outputs which may be used for further levels of look-ahead.

The Am2902 is generally used with the 2901 bipolar microprocessor unit to provide look-ahead over word lengths of more than four bits. The look-ahead carry generator can be used with binary ALU's in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

The logic equations provided at the outputs are:

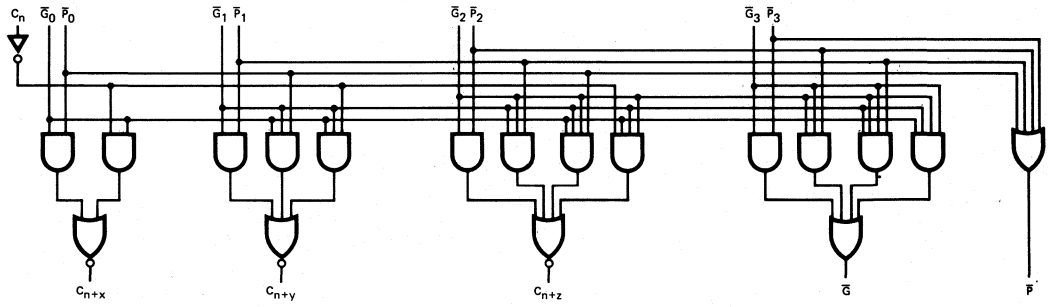
$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

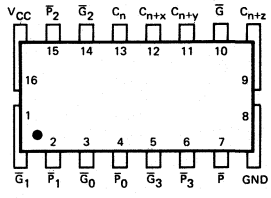
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2902PC
Hermetic DIP	0°C to +70°C	AM2902DC
Dice	0°C to +70°C	AM2902XC
Hermetic DIP	−55°C to +125°C	AM2902DM
Hermetic Flat Pack	−55°C to +125°C	AM2902FM
Dice	−55°C to +125°C	AM2902XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2902XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2902XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8mA V_{IN} = V_{IH} or V_{IL}		2.4	3.0		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −12mA				−1.5	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	C_n			−3.2	mA
			$\overline{P}_3$			−4.8	
			$\overline{P}_2$			−6.4	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			−8.0	
			$\overline{G}_0, \overline{G}_2$			−14.4	
			$\overline{G}_1$			−16	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V	C_n			80	μA
			$\overline{P}_3$			120	
			$\overline{P}_2$			160	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			200	
			$\overline{G}_0, \overline{G}_2$			360	
			$\overline{G}_1$			400	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. All Outputs LOW	MIL		62	99	mA
			COM'L		58	94	
		V_{CC} = MAX. All Ouputs HIGH	MIL		37		mA
			COM'L		35		

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current X Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS V_{CC} = 5.0V, T_A = 25°C, C_L = 15pF, R_L = 400Ω

Parameter	From (Input)	To (Output)	Test Figure	Test Conditions	Min	Typ	Max	Units
t_{PLH}	C_n	C_{n+j}	2	$\overline{P}_0 = \overline{P}_1 = \overline{P}_2 = 0$ V $\overline{G}_0 = \overline{G}_1 = \overline{G}_2 = 4.5$ V		11	14	ns
t_{PHL}						11	14	
t_{PLH}	$\overline{P}_i$	C_{n+j}	3	$\overline{P}_i = 0$ V (j > i) $C_n = \overline{G}_0 = \overline{G}_1 = \overline{G}_2 = 4.5$ V		6.0	8.0	ns
t_{PHL}						6.0	8.0	
t_{PLH}	$\overline{G}_i$	C_{n+j}	3	$\overline{G}_i = 0$ V (j > i) $C_n = \overline{P}_0 = \overline{P}_1 = \overline{P}_2 = 4.5$ V		8.0	10	ns
t_{PHL}						8.0	10	
t_{PLH}	$\overline{P}_i$	$\overline{G}$ or $\overline{P}$	2	$\overline{P}_i = 0$ V (j > i) $C_n = \overline{G}_0 = \overline{G}_1 = \overline{G}_2 = 4.5$ V		11	14	ns
t_{PHL}						11	14	
t_{PLH}	$\overline{G}_i$	$\overline{G}$ or $\overline{P}$	2	$\overline{G}_i = 0$ V (j > i) $C_n = \overline{P}_0 = \overline{P}_1 = \overline{P}_2 = 4.5$ V		12	14	ns
t_{PHL}						12	14	

DEFINITION OF FUNCTIONAL TERMS

C_n Carry-in. The carry-in input to the look-ahead generator. Also the carry-in input to the nth Am2901 microprocessor ALU input.

C_{n+j} Carry-out. (j = x, y, z). The carry-out output to be used at the carry-in inputs of the n+1, n+2 and n+3 microprocessor ALU slices.

G_i, P_i Generate and propagate inputs respectively (i = 0, 1, 2, 3). The carry generate and carry propagate inputs from the n, n+1, n+2 and n+3 microprocessor ALU slices.

G, P Generate and propagate outputs respectively. The carry generate and carry propagate outputs that can be used with the next higher level of carry look-ahead if used.

TRUTH TABLE

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	H	H	H					L		
X	X	H	H	H	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	L	X	L	X					L		
X	L	X	X	L	X	X					L		
H	X	L	X	L	X	L					L		
X		X	X	X	X	H	H	H				H	
X		X	X	H	H	H	H	X				H	
X		X	H	H	X	X	H	X				H	
H		X	H	H	X	X	H	X				H	
X		X	X	X	X	X	L	X				L	
X		X	X	X	L	X	X	L				L	
X		X	L	X	L	X	X	L				L	
L		X	X	L	X	L	X	L				L	
H		X		X		X		X					H
X		X		H		X		X					H
X		X		X		H		X					H
X		X		X		X		H					H
X		X		L		L		L					L

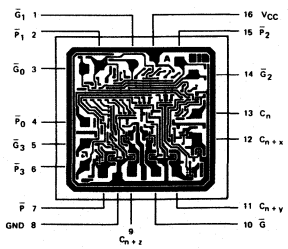
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{G}_1$	1	8.0	–	–
$\overline{P}_1$	2	4.0	–	–
$\overline{G}_0$	3	7.2	–	–
$\overline{P}_0$	4	4.0	–	–
$\overline{G}_3$	5	4.0	–	–
$\overline{P}_3$	6	2.4	–	–
$\overline{P}$	7	–	16	8
GND	8	–	–	–
C_{n+z}	9	–	16	8
$\overline{G}$	10	–	16	8
C_{n+y}	11	–	16	8
C_{n+x}	12	–	16	8
C_n	13	1.6	–	–
$\overline{G}_2$	14	7.2	–	–
$\overline{P}_2$	15	3.2	–	–
V_{CC}	16	–	–	–

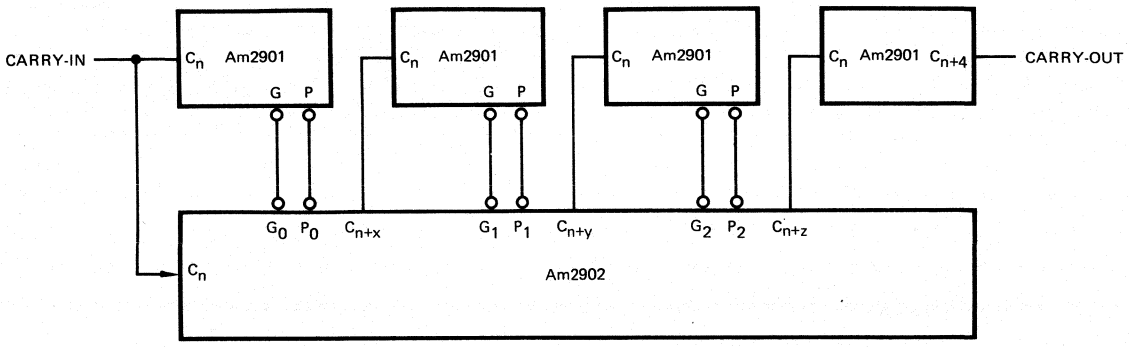
A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

Metallization and Pad Layout

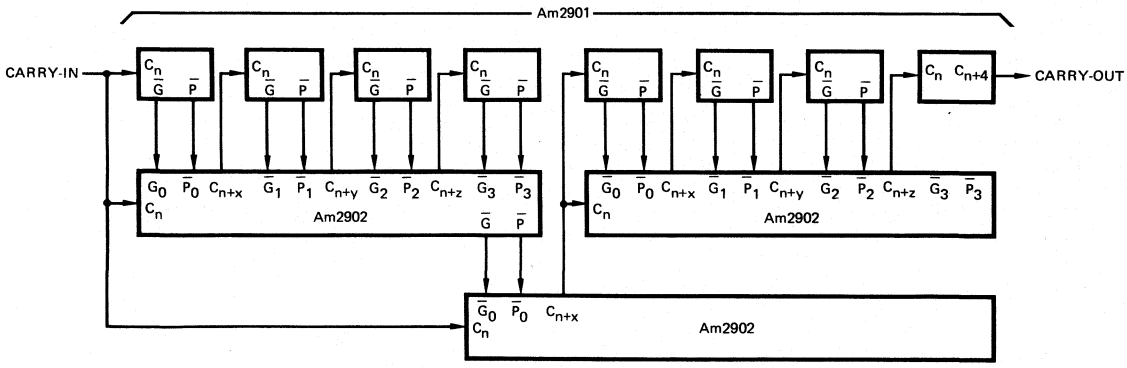


DIE SIZE 0.068" X 0.068"

APPLICATIONS



16-BIT CARRY LOOK-AHEAD CONNECTION.



32-BIT ALU, THREE LEVEL CARRY LOOK-AHEAD.

Am2905

Quad Two-Input OC Bus Transceiver With Three-State Receiver

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 100 mA at 0.8V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

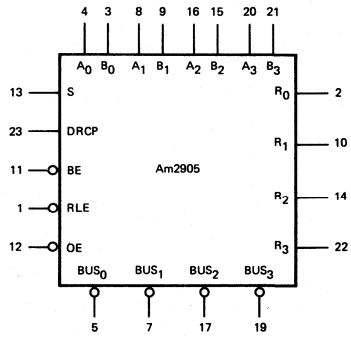
The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

ORDERING INFORMATION

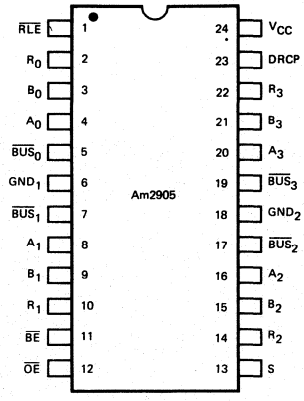
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2905PC
Hermetic DIP	0°C to +70°C	AM2905DC
Dice	0°C to +70°C	AM2905XC
Hermetic DIP	–55°C to +125°C	AM2905DM
Hermetic Flat Pak	–55°C to +125°C	AM2905FM
Dice	–55°C to +125°C	AM2905XM

LOGIC SYMBOL



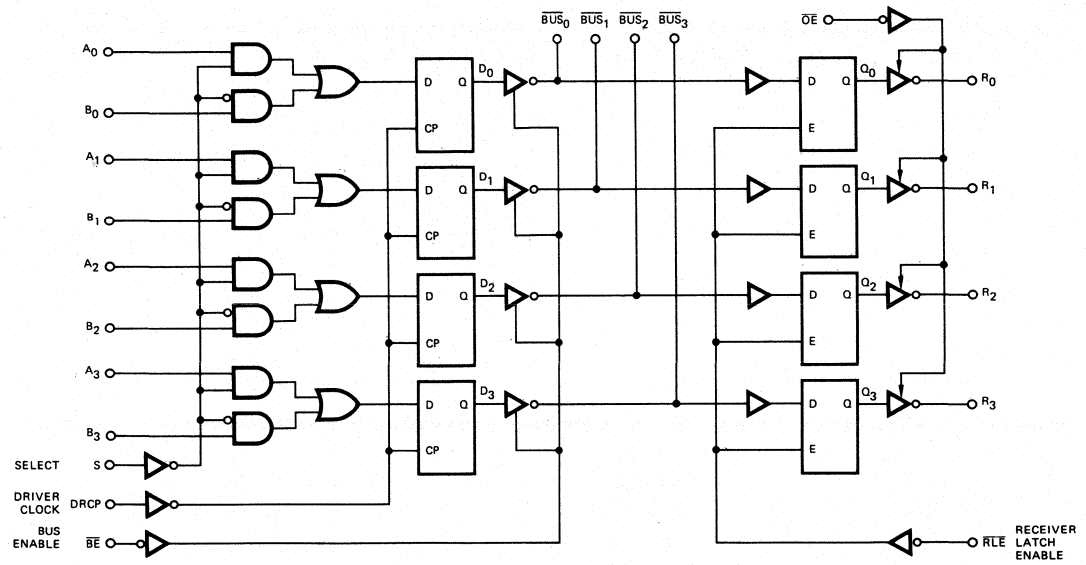
V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V
Am2905XM (MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2905XM MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

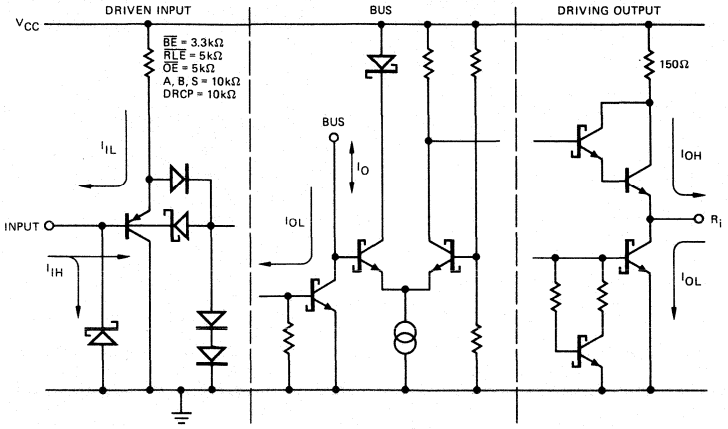
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	$V_{CC} = V_{IN}$, $V_{IN} = V_{IL}$ or V_{IH}	MIL, $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6$mA	2.4	3.4		
V_{OL}	Receiver Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4mA		0.27	0.4	Volts
			I_{OL} = 8mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.5	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5V				100	μA
I_O	Receiver Off-State Output Current	V_{CC} = MAX.	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	
I_{SC}	Receiver Output Short Circuit Current	V_{CC} = MAX.		−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND			69	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2905XM Min.	Am2905XM Typ. (Note 2)	Am2905XM Max.	Am2905XC Min.	Am2905XC Typ. (Note 2)	Am2905XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Input (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{ZH}	Output Control to Receiver Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Receiver Output			14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

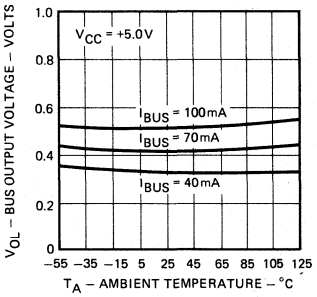
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



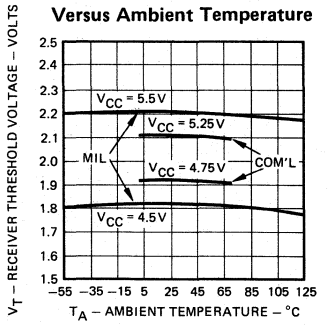
Note: Actual current flow direction shown.

TYPICAL PERFORMANCE CURVES

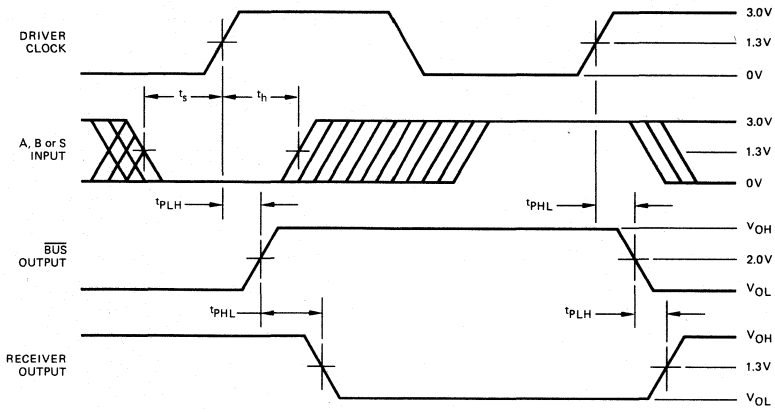
Bus Output Low Voltage Versus Ambient Temperature



Receiver Threshold Variation Versus Ambient Temperature



SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW-to-HIGH transition

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 — The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 — The "B" word data input into the two input multiplexers of the driver register.

S — Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP — Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ — Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

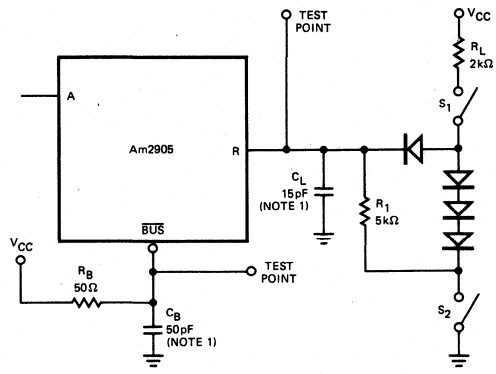
$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$ — The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 — The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

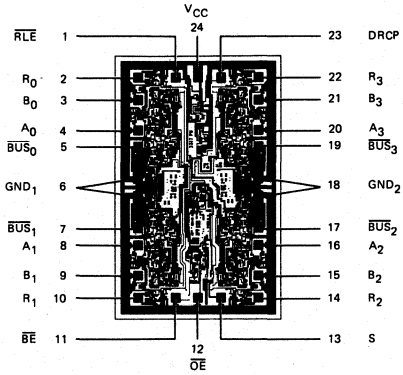
$\overline{RLE}$ — Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ — Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT

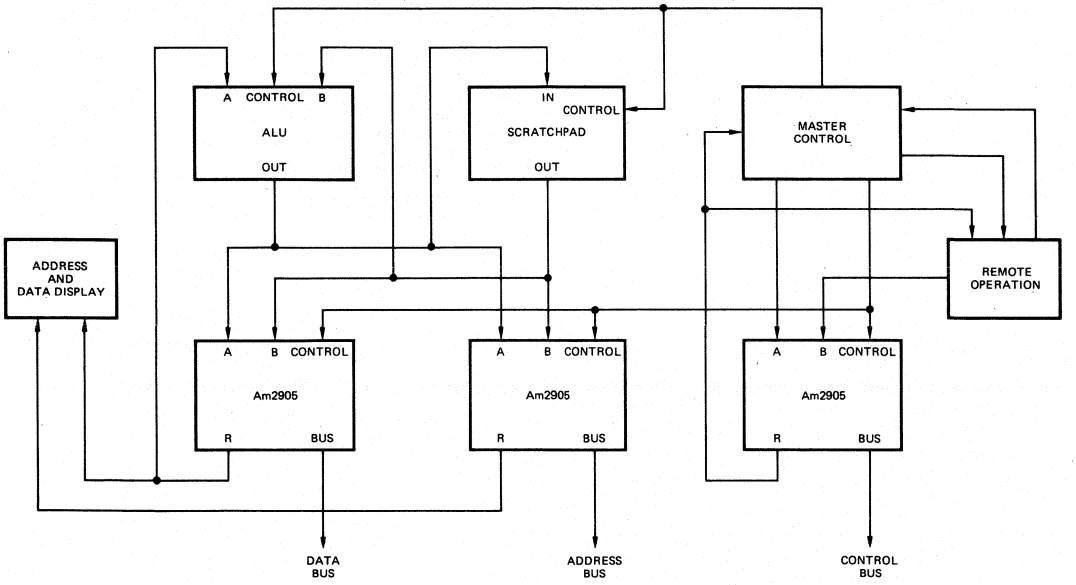


Metallization and Pad Layout

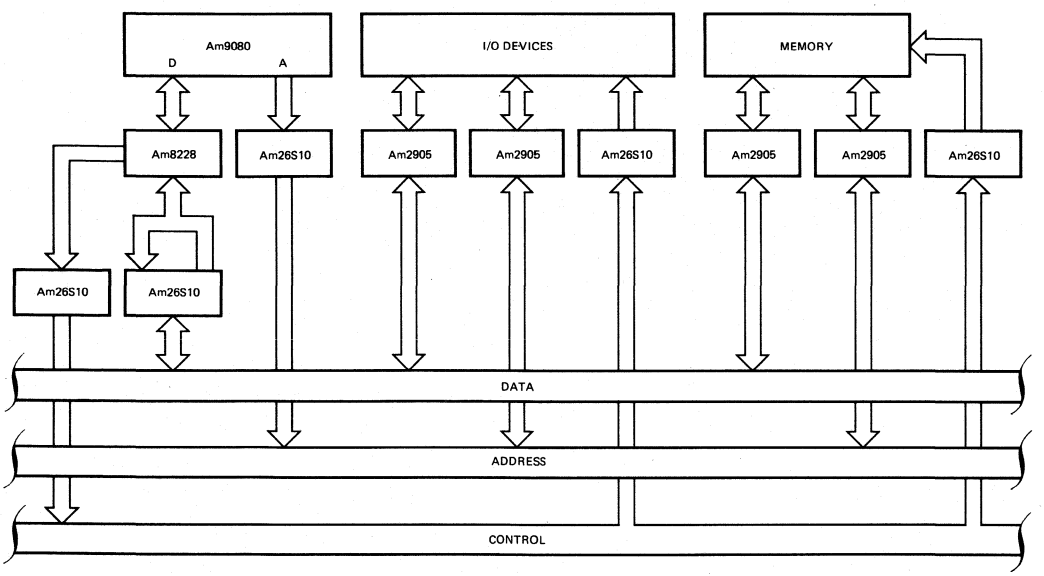


DIE SIZE 0.080" X 0.130"

APPLICATIONS



The Am2905 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.



Using the Am2905 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

Am2906

Quad Two-Input OC Bus Transceiver With Parity

Distinctive Characteristics

- Quad high-speed LSI bus transceiver.
- Open-collector bus driver.
- Two-port input to D-type register on driver.
- Bus driver output can sink 100 mA at 0.8V max.
- Internal odd 4-bit parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.
- Advanced low-power Schottky processing.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

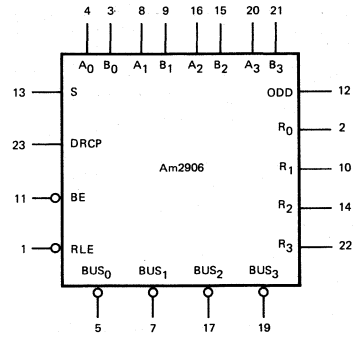
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

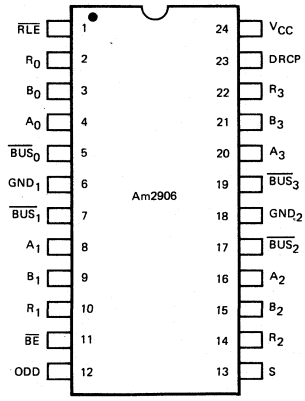
The Am2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

CONNECTION DIAGRAM
Top View

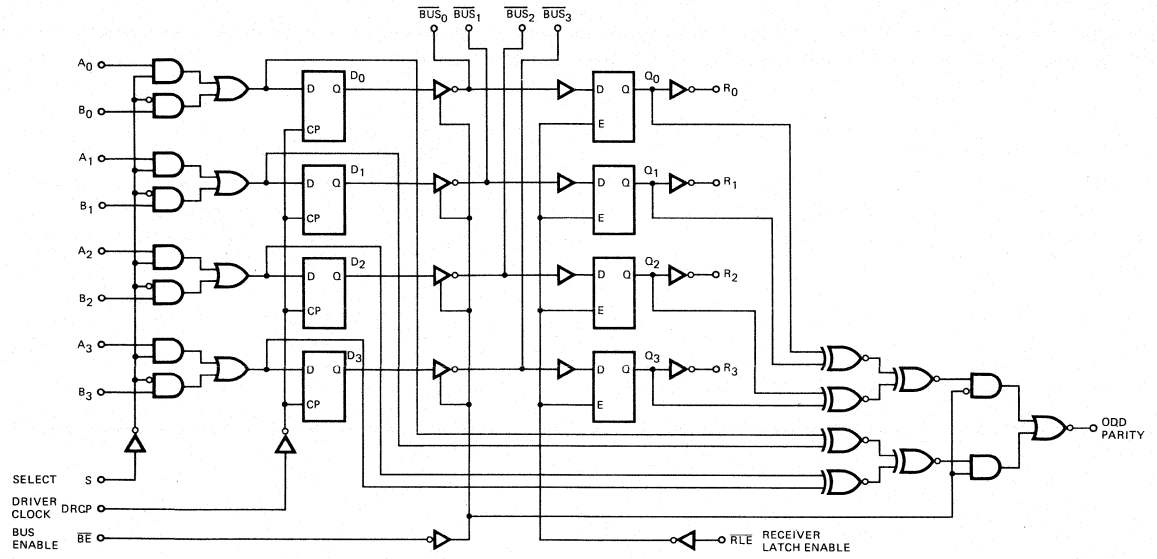


Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2906PC
Hermetic DIP	0°C to +70°C	AM2906DC
Dice	0°C to +70°C	AM2906XC
Hermetic DIP	−55°C to +125°C	AM2906DM
Hermetic Flat Pak	−55°C to +125°C	AM2906FM
Dice	−55°C to +125°C	AM2906XM

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage		I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	$T_A = 0°C$ to $+70°C$	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	$T_A = -55°C$ to $+125°C$	V_{CC} MIN. 4.5V	V_{CC} MAX. = 5.5V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

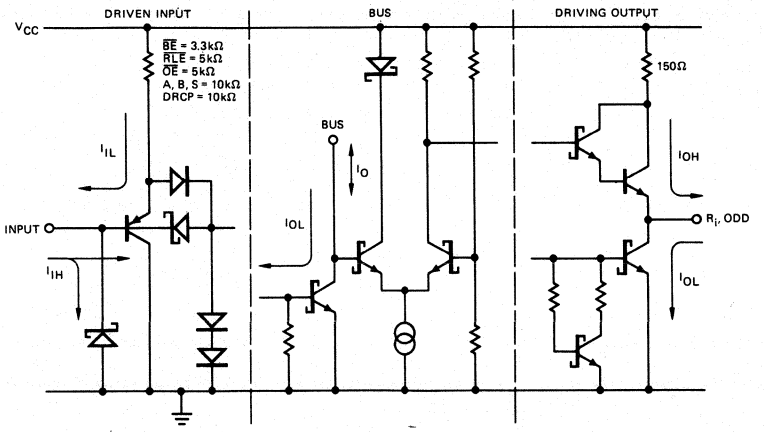
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL	$I_{OH} = -1mA$	2.4	3.4		Volts
			COM'L	$I_{OH} = -2.6mA$	2.4	3.4		
	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4mA$			0.27	0.4	Volts
			$I_{OL} = 8mA$			0.32	0.45	
			$I_{OL} = 12mA$			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5V$					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND				72	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2906XM Min.	Am2906XM Typ. (Note 2)	Am2906XM Max.	Am2906XC Min.	Am2906XC Typ. (Note 2)	Am2906XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L(BUS) = 50pF, R_L(BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Inputs (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

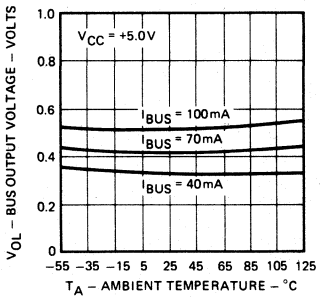
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



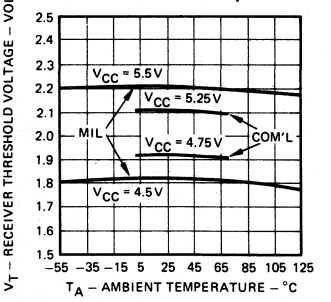
Note: Actual current flow direction shown.

TYPICAL PERFORMANCE CURVES

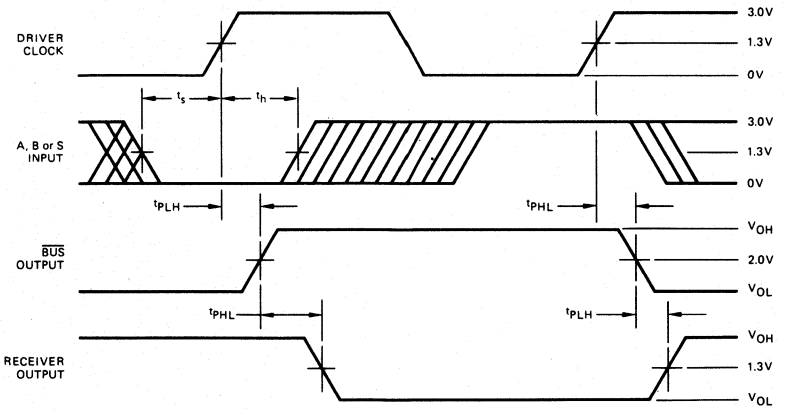
Bus Output Low Voltage Versus Ambient Temperature



Receiver Threshold Variation Versus Ambient Temperature



SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH, L = LOW; Z = HIGH Impedance, NC = No change; X = Don't care, ↑ = LOW-to-HIGH transition; i = 0, 1, 2, 3

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 — The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 — The "B" word data input into the two input multiplexers of the driver register.

S — Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP — Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ — Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

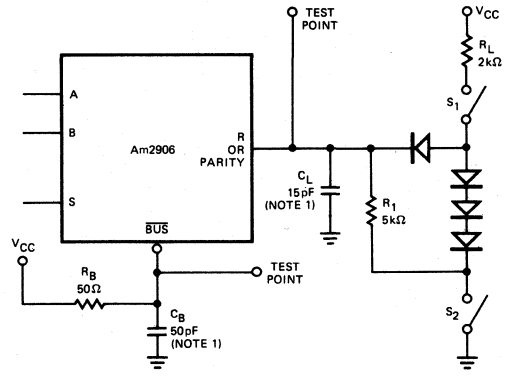
$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$ — The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 — The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

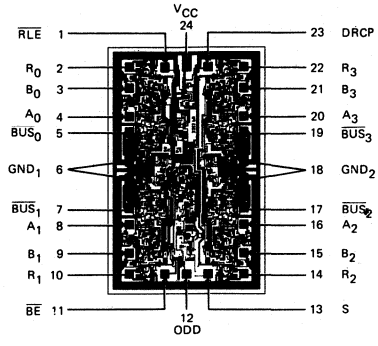
$\overline{RLE}$ — Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ — Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT

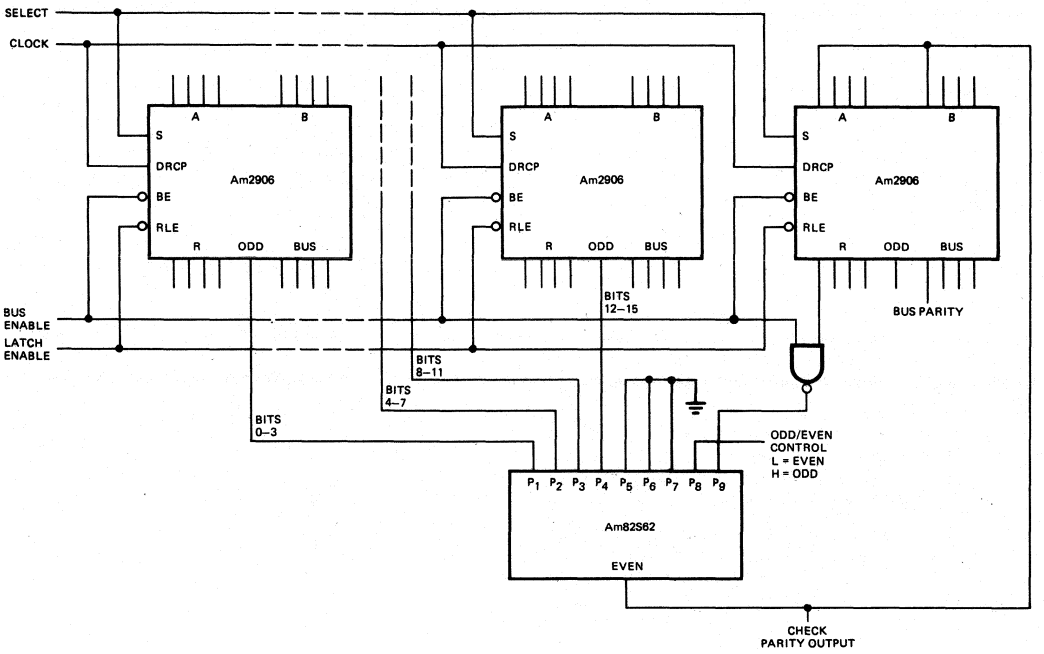


Metallization and Pad Layout

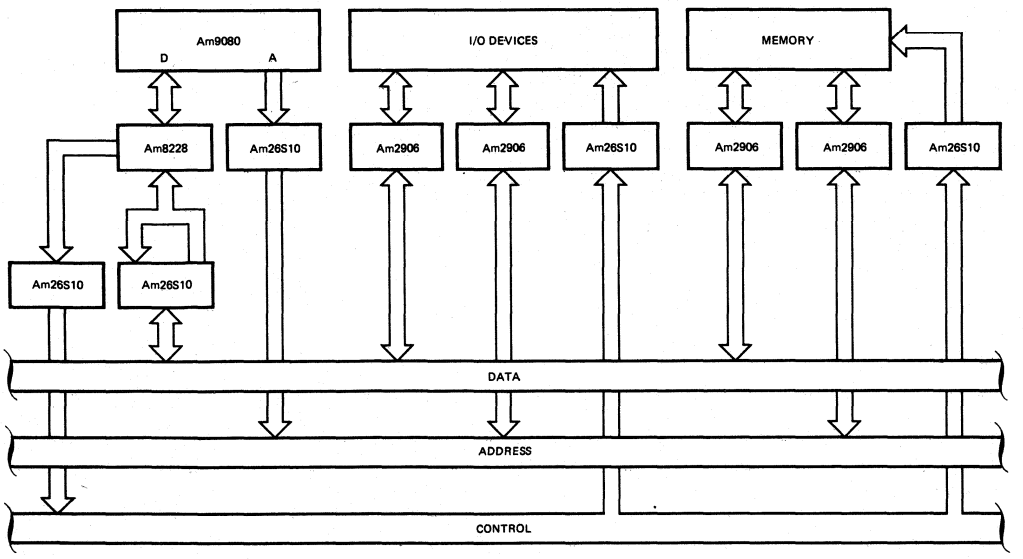


DIE SIZE 0.080" X 0.130"

APPLICATIONS



Generating or checking parity for 16 data bits.



Using the Am2906 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

Am2907

Quad Bus Transceiver With Three-State Receiver And Parity

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- D-type register on driver
- Bus driver output can sink 100 mA at 0.8 V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2907 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

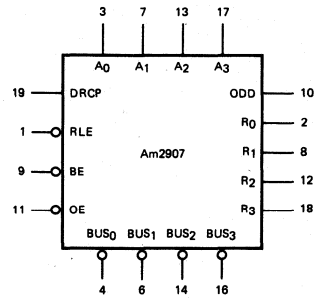
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8 V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2907 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

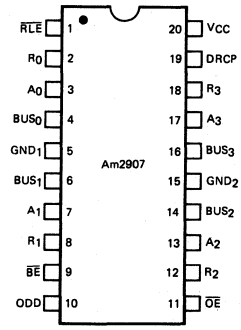
LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

CONNECTION DIAGRAMS
Top Views

DIP



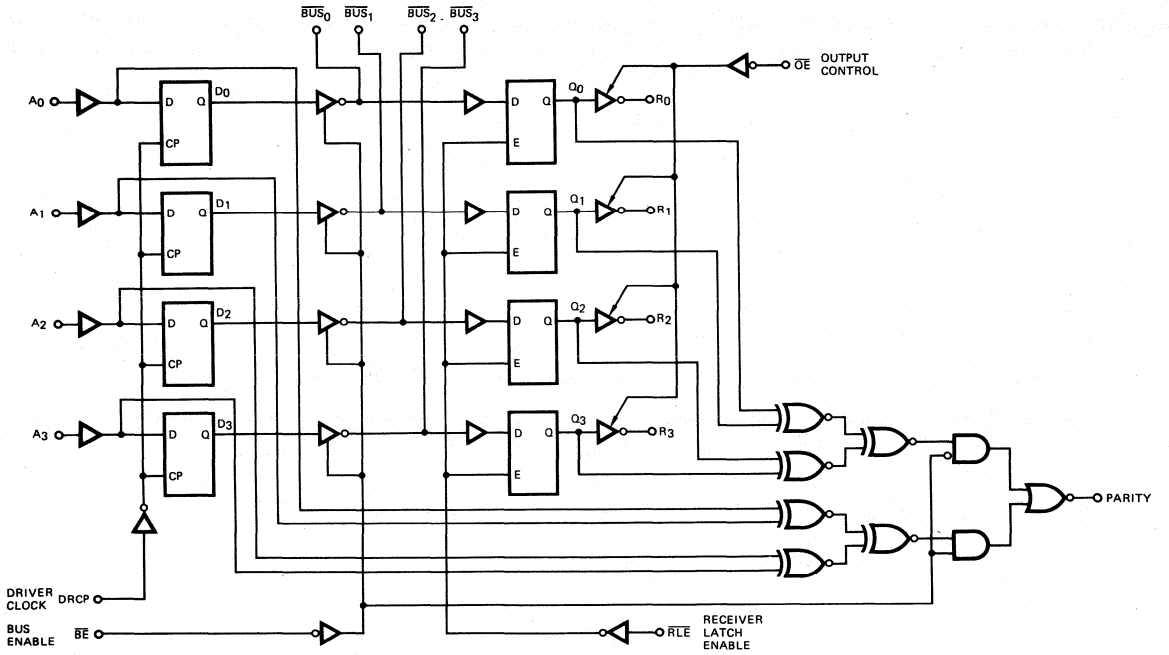
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2907PC
Hermetic DIP	0°C to +70°C	AM2907DC
Dice	0°C to +70°C	AM2907XC
Hermetic DIP	−55°C to +125°C	AM2907DM
*Hermetic Flat Pak	−55°C to +125°C	AM2907FM
Dice	−55°C to +125°C	AM2907XM

*Available on special order

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	200 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2907XM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	µA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2907XM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

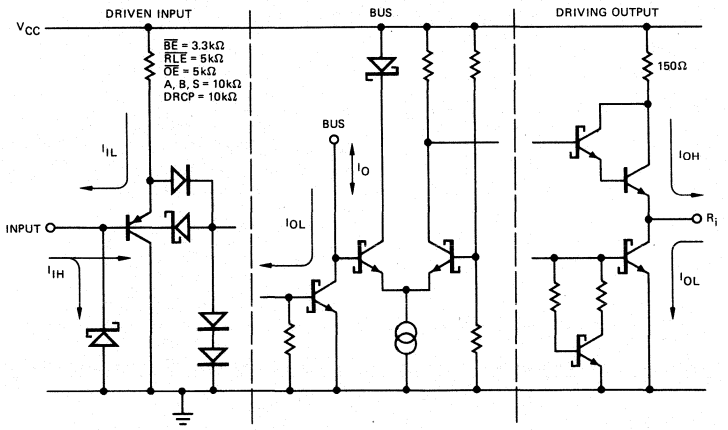
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1mA$		2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6mA$		2.4	3.4		
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4mA			0.27	0.4	Volts
			I_{OL} = 8mA			0.32	0.45	
			I_{OL} = 12mA			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5 V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND				75	110	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V				20	μA
			V_O = 0.4 V				−20	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2907XM Min.	Am2907XM Typ. (Note 2)	Am2907XM Max.	Am2907XC Min.	Am2907XC Typ. (Note 2)	Am2907XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	A Data Inputs	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{ZH}	Output Control to Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Output	C_L = 5.0pF, R_L = 2.0kΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

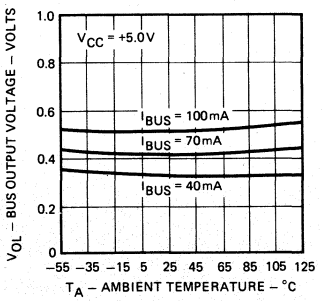
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



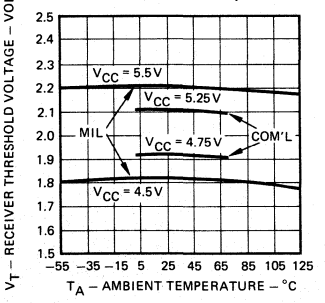
Note: Actual current flow direction shown.

TYPICAL PERFORMANCE CURVES

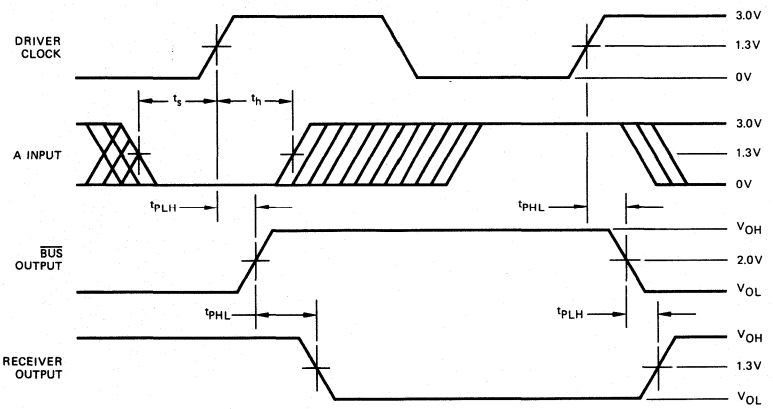
Bus Output Low Voltage Versus Ambient Temperature



Receiver Threshold Variation Versus Ambient Temperature



SWITCHING WAVEFORMS



Note: Bus to Reciever output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

TRUTH TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	B_i	R_i	
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

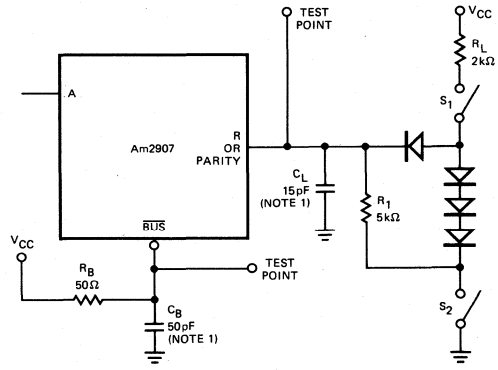
R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

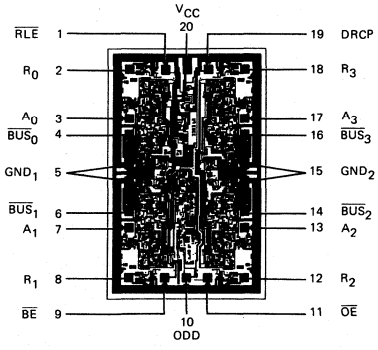
ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT

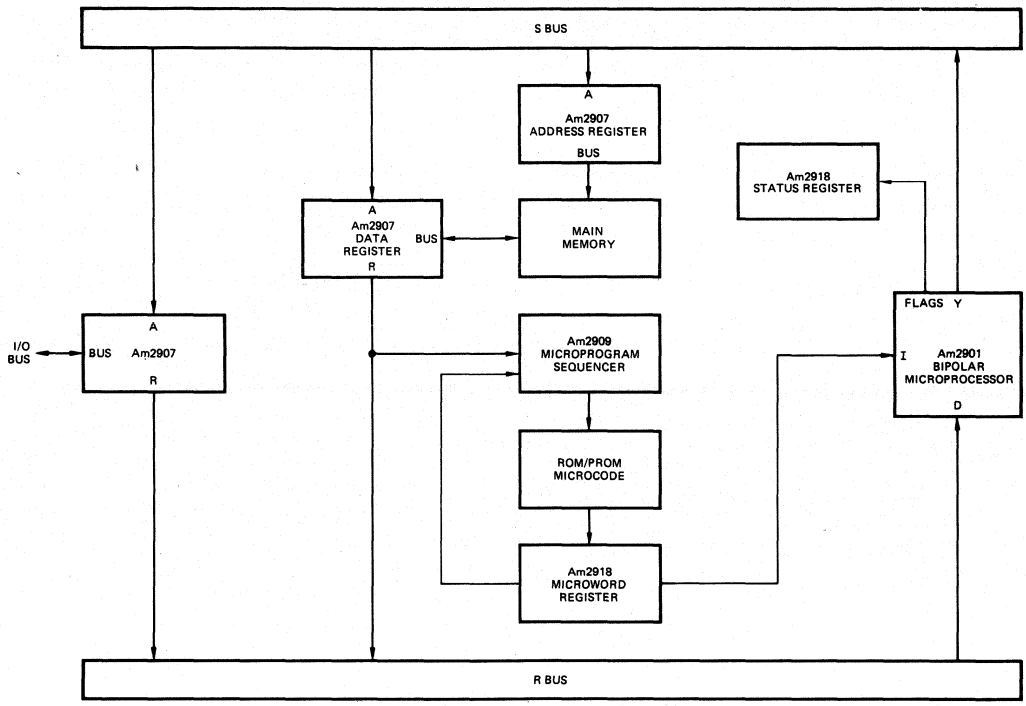


Metallization and Pad Layout

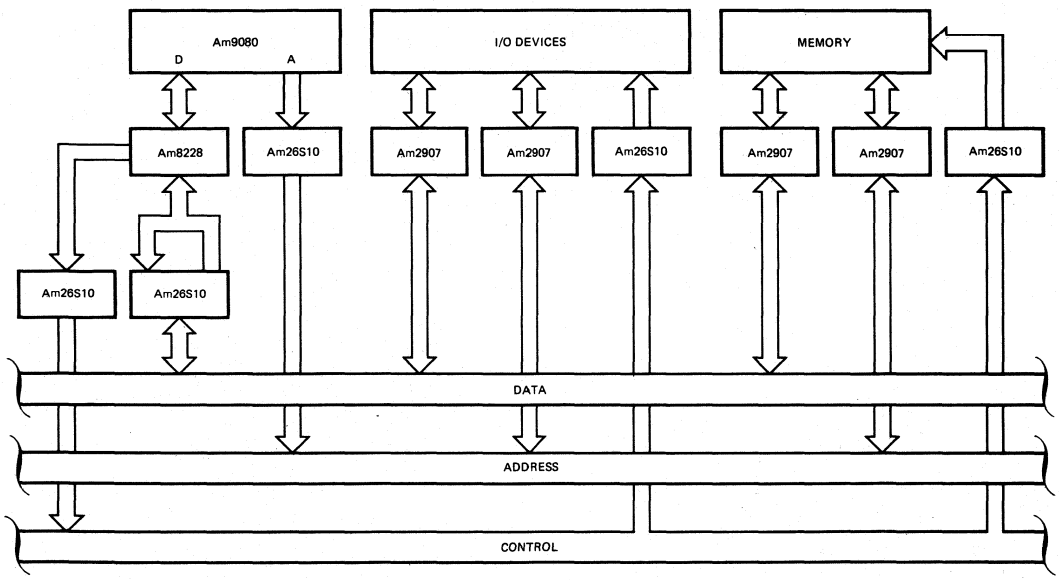


DIE SIZE 0.080" X 0.130"

APPLICATIONS



The Am2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.



Using the Am2907 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

Am2909 • Am2911

Microprogram Sequencers

DISTINCTIVE CHARACTERISTICS

- 4-bit slice cascadable to any number of microwords
- Internal address register
- Branch input for N-way branches
- Cascadable 4-bit microprogram counter
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines.
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions (Am2909 only).
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock
- Am2909 in 28-pin package
- Am2911 in 20-pin package

GENERAL DESCRIPTION

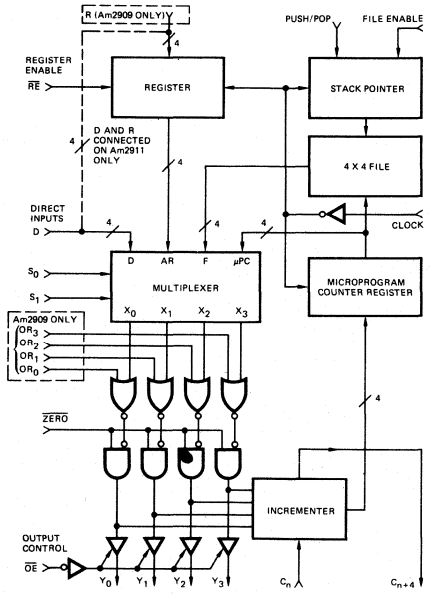
The Am2909 is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two Am2909's may be interconnected to generate an eight-bit address (256 words), and three may be used to generate a twelve-bit address (4K words).

The Am2909 can select an address from any of four sources. They are: 1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a four-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The Am2911 is an identical circuit to the Am2909, except the four OR inputs are removed and the D and R inputs are tied together. The Am2911 is in a 20-pin, 0.3" centers package.

TABLE OF CONTENTS

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



ARCHITECTURE OF THE Am2909/Am2911

The Am2909/Am2911 are bipolar microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256-words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 2.

The device contains a four-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S_0 and S_1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a four-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the Am2911, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The Am2909/Am2911 contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out (C_{n+4}) such that cascading to larger word lengths is straightforward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y+1→μPC.) Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle (Y→μPC). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last source available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage — the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops or stack references can be achieved. One microinstruction subroutines can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The Am2909/Am2911 feature three-state Y outputs. These can be particularly useful in military designs requiring external Ground Support Equipment (GSE) to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/PROM.

PHYSICAL DIMENSIONS

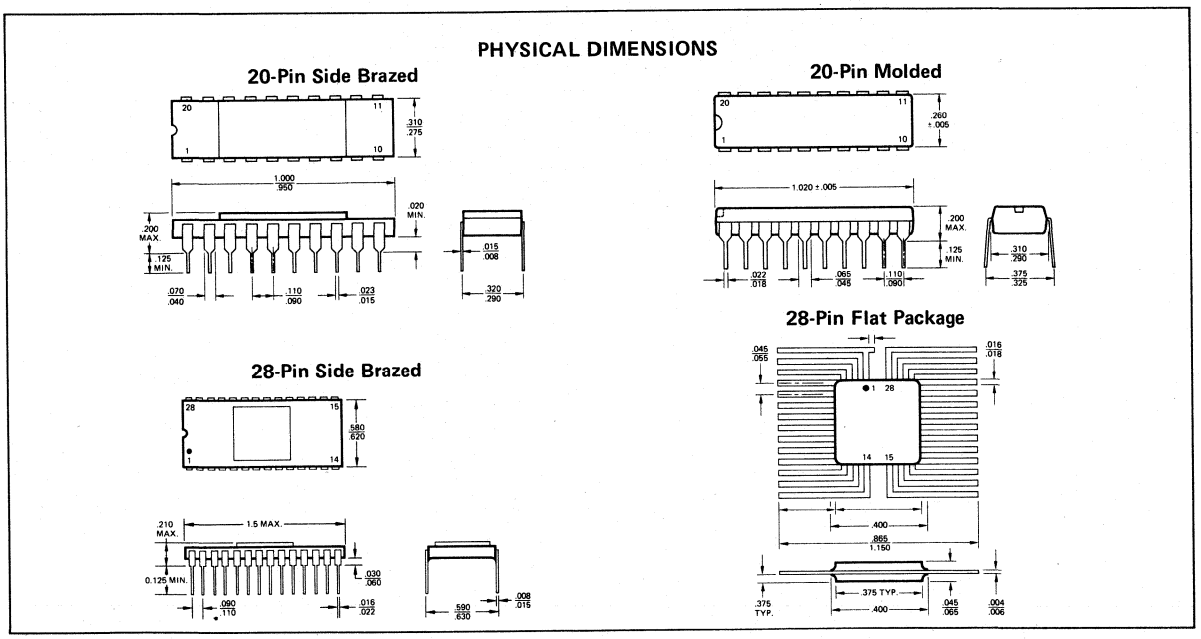
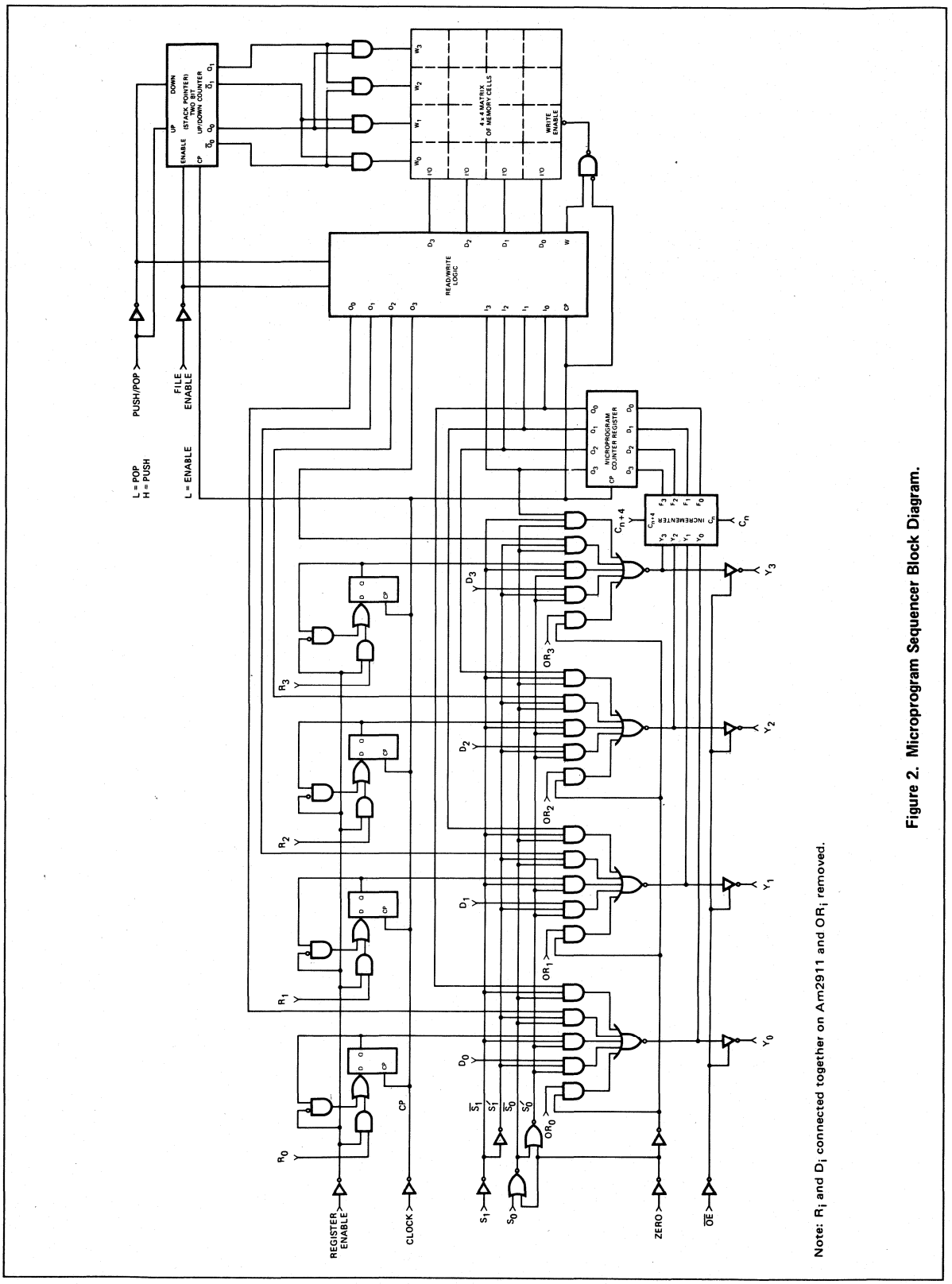


Figure 1.



Note: R_i and D_i connected together on Am2911 and OR_i removed.

Figure 2. Microprogram Sequencer Block Diagram.

DEFINITION OF TERMS

A set of symbols is used in this data sheet to represent various internal and external registers and signals used with the Am2909. Since its principle application is as a controller for a microprogram store, it is necessary to define some signals associated with the microcode itself. Figure 3 illustrates the basic interconnection of Am2909, memory, and microinstruction register. The definitions here apply to this architecture.

Inputs to Am2909/Am2911

S_1, S_0	Control lines for address source selection
$\overline{FE}$, PUP	Control lines for push/pop stack
$\overline{RE}$	Enable line for internal address register
OR_i	Logic OR inputs on each address output line
$\overline{ZERO}$	Logic AND input on the output lines
$\overline{OE}$	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance)
C_n	Carry-in to the incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock input to the AR and μPC register and Push-Pop stack

Outputs from the Am2909/Am2911

Y_i	Address outputs from Am2909. (Address inputs to control memory.)
C_{n+4}	Carry out from the incrementer

Internal Signals

μPC	Contents of the microprogram counter
REG	Contents of the register
STK0-STK3	Contents of the push/pop stack. By definition, the word in the four-by-four file, addressed by the stack pointer is STK0. Conceptually data is pushed into the stack at STK0; a subsequent push moves STK0 to STK1; a pop implies STK3 → STK2 → STK1 → STK0. Physically, only the stack pointer changes when a push or pop is performed. The data does not move. I/O occurs at STK0.
SP	Contents of the stack pointer

External to the Am2909/Am2911

A	Address to the control memory
I(A)	Instruction in control memory at address A
μWR	Contents of the microword register (at output of control memory). The microword register contains the instruction currently being executed.
T_n	Time period (cycle) n

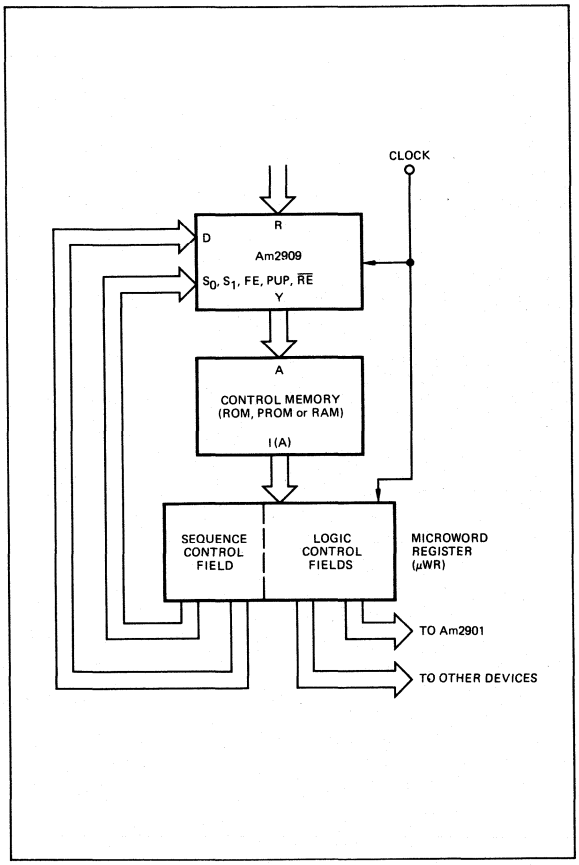


Figure 3. Microprogram Sequencer Control.

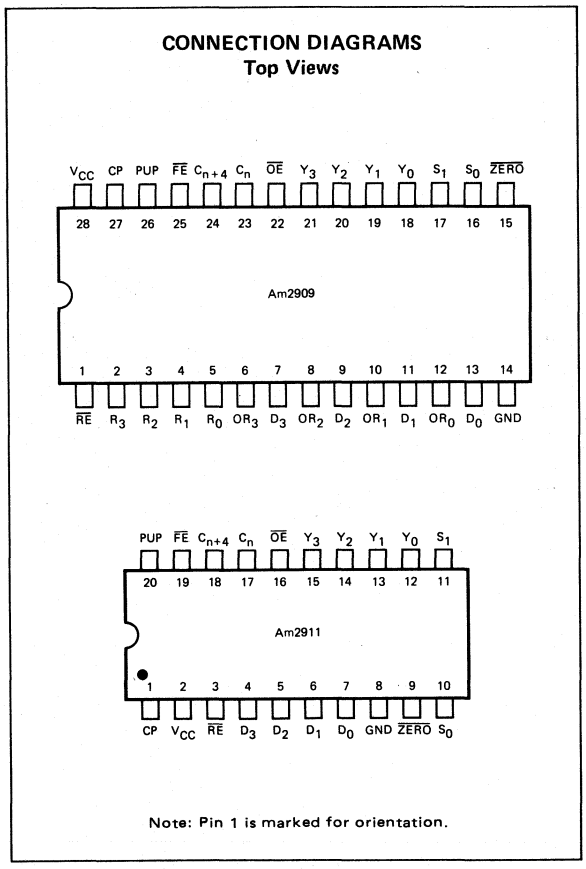


Figure 4.

OPERATION OF THE Am2909/Am2911

Figure 5 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Figure 5 also shows the truth table for the output control and for the control of the push/pop stack. Figure 6 shows in detail the effect of S_0, S_1, $\overline{FE}$ and PUP on the Am2909. These four signals define what address appears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

Address Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPC
1	L	H	Register	REG
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 5.

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N N+1	0 0 0 0 –	J J+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	J –	Pop Stack	End Loop
N N+1	0 0 0 1 –	J J+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	J –	Push μPC	Set-up Loop
N N+1	0 0 1 X –	J J+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	J –	Continue	Continue
N N+1	0 1 0 0 –	J K+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	K –	Pop Stack; Use AR for Address	End Loop
N N+1	0 1 0 1 –	J K+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	K –	Push μPC; Jump to Address in AR	JSR AR
N N+1	0 1 1 X –	J K+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	K –	Jump to Address in AR	JMP AR
N N+1	1 0 0 0 –	J Ra+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	Ra –	Jump to Address in STK0; Pop Stack	RTS
N N+1	1 0 0 1 –	J Ra+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	Ra –	Jump to Address in STK0; Push μPC	
N N+1	1 0 1 X –	J Ra+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	Ra –	Jump to Address in STK0	Stack Ref (Loop)
N N+1	1 1 0 0 –	J D+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	D –	Pop Stack; Jump to Address on D	End Loop
N N+1	1 1 0 1 –	J D+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	D –	Jump to Address on D; Push μPC	JSR D
N N+1	1 1 1 X –	J D+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	D –	Jump to Address on D	JMP D

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH
Note: STK0 is the location addressed by the stack pointer.

Figure 6. Output and Internal Next-Cycle Register States for Am2909/Am2911.

Figure 7 illustrates the execution of a subroutine using the Am2909. The configuration of Figure 3 is assumed. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls (indirectly, perhaps) the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the Am2909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J+2, the sequence control portion of the microinstruction contains the comand "Jump to subroutine at A". At the time T_2, this instruction is in the μWR, and the Am2909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J+3 is pushed onto the stack. The return instruction is executed at T_5. Figure 8 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J−1	—
T_0	J	—
T_1	J+1	—
T_2	J+2	JSR A
T_6	J+3	—
T_7	J+4	—
	—	—
	—	—
	—	—
	—	—
	—	—
T_3	A	I(A)
T_4	A+1	—
T_5	A+2	RTS
	—	—
	—	—
	—	—
	—	—
	—	—
	—	—
	—	—

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	—	—	—	J+3	J+3	J+3	—	—		
	STK1	—	—	—	—	—	—	—	—		
	STK2	—	—	—	—	—	—	—	—		
	STK3	—	—	—	—	—	—	—	—		
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)		

Figure 7. Subroutine Execution.

C_n = HIGH

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J−1	—
T_0	J	—
T_1	J+1	—
T_2	J+2	JSR A
T_9	J+3	—
	—	—
	—	—
	—	—
	—	—
T_3	A	—
T_4	A+1	—
T_5	A+2	JSR B
T_7	A+3	—
T_8	A+4	RTS
	—	—
	—	—
	—	—
	—	—
T_6	B	RTS
	—	—
	—	—

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	—	—	—	J+3	J+3	J+3	A+3	J+3	J+3	—
	STK1	—	—	—	—	—	—	J+3	—	—	—
	STK2	—	—	—	—	—	—	—	—	—	—
	STK3	—	—	—	—	—	—	—	—	—	—
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)

Figure 8. Two Nested Subroutines. Routine B is Only One Instruction.

C_n = HIGH

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

P/N	Ambient Temperature	V_{CC}
Am2909/2911DC, PC	0°C to +70°C	4.75V to 5.25V
Am2909/2911DM, FM	−55°C to +125°C	4.50V to 5.50V

STANDARD SCREENING

(Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Level	
			Am2909/Am2911PC, DC	Am2909/Am2911DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C 24-hour 150°C	100%	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B 10,000 G	100% *	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/cm^3	100% *	100%
Gross Leak	1014	C2 Fluorocarbon	100% *	100%
Electrical Test Subgroups 1 and 7	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 7
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 7

*Not applicable for Am2909PC or Am2911PC.

ADDITIONAL SCREENING FOR CLASS B PARTS

Step	MIL-STD-883 Method	Conditions	Level
			Am2909/Am2911DMB, FMB
Burn-In	1015	D 125°C 160 hours min.	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

ORDERING INFORMATION

Package Type	Temperature Range	Am2909 Order Number	Am2911 Order Number
Molded DIP	0°C to +70°C	AM2909PC	AM2911PC
Hermetic DIP	0°C to +70°C	AM2909DC	AM2911DC
Hermetic DIP	−55°C to +125°C	AM2909DM	AM2911DM
Hermetic Flat Pak	−55°C to +125°C	Am2909FM	—
Dice	0°C to +70°C	Am2909XC	—

GROUP A SUBGROUPS

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum Rated Temeperature
11	Switching	Minimum Rated Temperature

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL	I_{OH} = −1.0mA	2.4			Volts
			COM'L	I_{OH} = −2.6mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA (Note 5)				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	C_n				−1.08	mA
			Push/Pop, $\overline{OE}$				−0.72	
			Others (Note 6)				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n				40	μA
			Push/Pop				40	
			Others (Note 6)				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	C_n, Push/Pop				0.2	mA
			Others (Note 6)				0.1	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)				80	130	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.7V	V_{OUT} = 0.4V				−20	μA
I_{OZH}			V_{OUT} = 2.7V				20	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply GND to C_n, R_0, R_1, R_2, R_3, OR_0, OR_1, OR_2, OR_3, D_0, D_1, D_2, and D_3. Other inputs open. All outputs open. Measured after a LOW-to-HIGH clock transition.
5. The 12mA guarantee applies only to Y_0, Y_1, Y_2 and Y_3.
6. For the Am2911, D_i and R_i are internally connected. Loading is doubled (to same values as Push/Pop).

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

All parameters are guaranteed worst case over the operating voltage and temperature range for the device type. (Grade C = 0°C to +70°C, 4.75V to 5.25V; Grade M = −55°C to +125°C, 4.5V to 5.5V)

TABLE I
MINIMUM CLOCK REQUIREMENTS

Minimum Clock LOW Time	50
Minimum Clock HIGH Time	30

TABLE II
MAXIMUM COMBINATORIAL PROPAGATION DELAYS

OUTPUTS / INPUTS	Y_i	C_{n+4}
$\overline{OE}$	25	–
$\overline{ZERO}$	35	45
OR_i	20	32
S_0, S_1	40	50
D_i	20	32
C_n	–	18

TABLE III
MAXIMUM DELAYS FROM CLOCK TO OUTPUTS

FUNCTIONAL PATH	GRADE	CLOCK TO Y_i	CLOCK TO C_{n+4}
Register (S_1 S_0 = LH)	C	48	58
	M	55	65
μ Program Counter (S_1 S_0 = LL)	C	48	58
	M	55	65
File (S_1 S_0 = HL)	C	70	80
	M	80	90

R_L = 2.0kΩ C_L = 15pF

TABLE IV
SET-UP AND HOLD TIME REQUIREMENTS

EXTERNAL INPUTS	t_s	t_h
$\overline{RE}$	20	5.0
R_i	15	0
PUSH/POP	20	5.0
$\overline{FE}$	20	0
C_n	15	0
D_i	20	0
OR_i	20	0
S_0, S_1	40	0
$\overline{ZERO}$	40	0

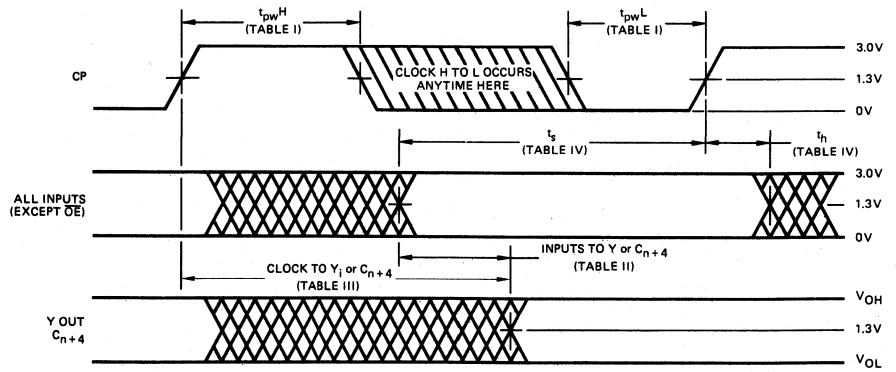


Figure 12. Switching Waveforms. See Tables for Specific Values.

A COMPUTER CONTROL UNIT USING THE Am2909

By James R. W. Clymer

INTRODUCTION

The computer control unit (CCU) is generally the single most complicated subsystem in today's digital computer. A CCU is complicated from the conceptualization, design and implementation viewpoints, because it is the subsystem that controls the internal buses and subsystems of the processor, synchronizes internal and external events and grants or denies permission to external systems. The Am2909 Microprogram Sequencer is an excellent mechanism for simplifying the CCU design task.

COMPUTER ARCHITECTURE

A classical computer architecture is shown in Figure 1. The data bus is commonly used by all of the subsystems in the computer. Information, instructions, address operands, data and sometimes control signals are transmitted down the data bus under control of a microprogram. The microprogram selects the source of the data as well as the destination (s) of the data. In a more complicated system there may be a number of data buses.

The address bus is typically used to select a word in memory for an internal computer function, or to select an input/output port for an external subsystem or peripheral function. Also selected by microprogram command, the source of the data for the address bus may be the program counter, the memory address register, a direct memory address controller, an interface controller etc.

The arithmetic/logic unit (ALU) is actually that portion of the processor that computes. Depending upon the complexity of the ALU, a large number of different arithmetic functions can be accomplished in various number system using different representations of those data. The most common minimum set, however, are the functions (A plus B), (A minus B) and (B

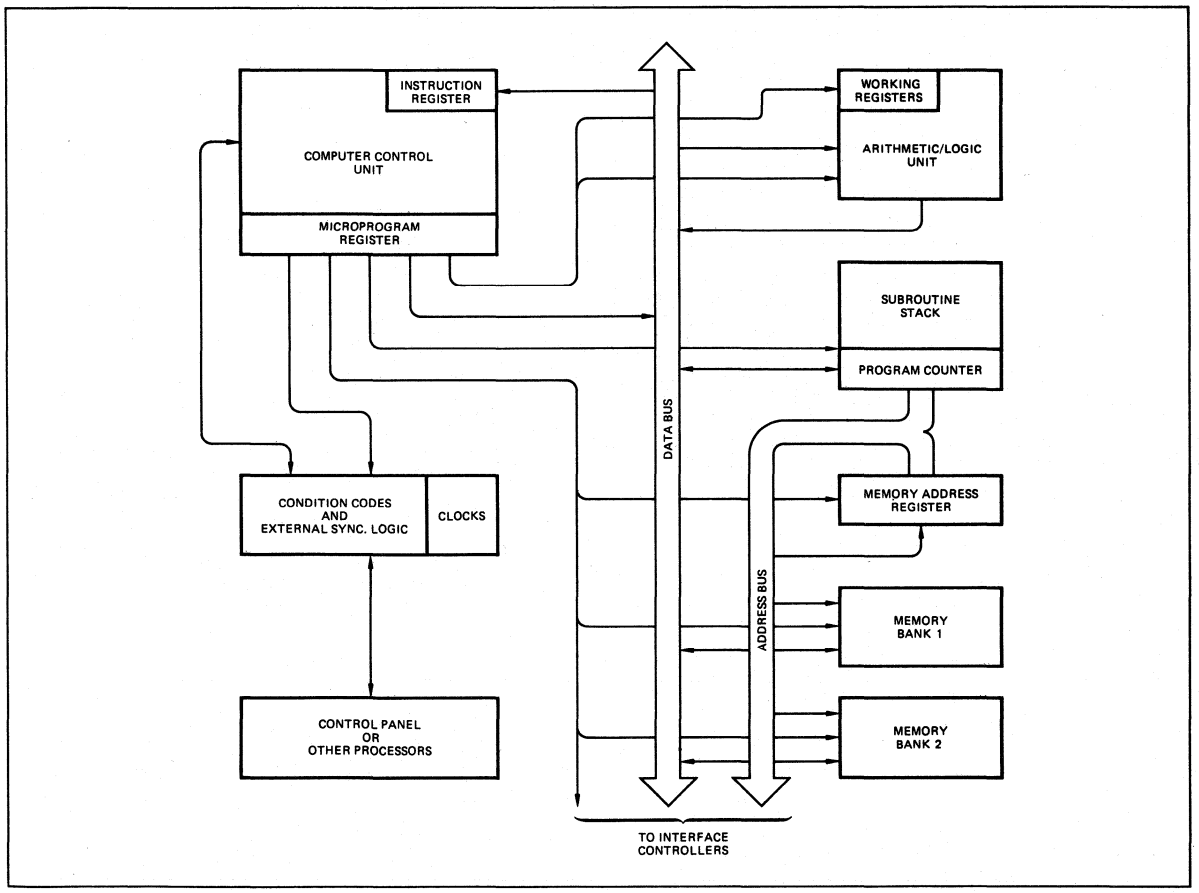


Figure 1. Generalized Computer Architecture.

minus A) performed in fixed point, two's complement binary form; where A and B are the ALU inputs. The logical functions are obtained from the same combinatorial logic array that is used for the arithmetic functions, but it is gated in a different manager. The minimum logical function capability will be (A OR B), (A AND B) and (A EXCLUSIVE-OR B). In addition to these combinatorial logic functions, there are sets of shift and rotate instructions that complete the basic instruction set.

The ALU provides a set of condition codes as a result of the current arithmetic or logical function. These condition codes include such variables as carry out, A = B, the sign bit, result equals zero, etc. The condition codes, along with other computer status information, are stored in a register for later use by the programmer or computer control unit.

Third generation processors also provide for a general-purpose register set that is available to the programmer to be used to hold variables that are used often — passing arguments to subroutines, referencing memory indirectly etc. Depending on the architecture of the machine, the general-purpose registers may be selected directly from the operands in the instruction register, from an address in the microprogram store, or one of the two sources as determined by a bit in the microprogram store.

The program counter and the memory address register are the two main sources of memory word and I/O address select data on the address bus. The program counter contains the address of the next instruction or instruction operand that is to be fetched from main memory, and the memory address register contains instruction address operands that are necessary to fetch the data required for the execution of the current instruction.

A subroutine address stack is provided to allow the return address linkage to be handled easily when exiting a subroutine. The address stack is a last-in, first-out stack that is controlled by a jump-to-subroutine, PUSH, or a return-from-subroutine, POP, instruction from the CCU microprogram word.

Main memory poses an interesting set of problems to computer designers. Random access memory is typically slower than the computer control unit or arithmetic logic unit speed. And, on the other hand, read only memory may be much faster than the control process. The same set of problems is presented to the system by peripheral devices and processes. The computer control unit contends with these problems as well as the problems of synchronizing asynchronous events.

THE CONTROL SEQUENCE

The computer control unit contains an instruction register, microprogram storage and usually a microprogram register. Figure 2 presents a state diagram for a typical computer control unit. The first state of any processor must be an initialization sequence, regardless of its level of complexity or sophistication. The purpose of the initialization sequence is to place all of the system control storage elements in a known state such that control of the process can be started in an orderly manner. For example, registers, condition code, flag, and carry/link flip-flops are either preset to logic "1" or cleared to logic "0". Sometimes a sequence of events takes place such as the initialization of sets of register stacks or main memory. Also because some peripheral equipment may be involved that may be damaged by randomly changing states at its interface, very close attention must be given to the initialization process within the CCU state machine. A further requirement of this initialization process is that clock pulses must be withheld from the initialized hardware in some manner until the initialization procedure is completed.

The initialization sequence is usually started by one of three events: application of primary power to the system; either a programmed or operator generated "Master Reset" command; or an error that the state machine cannot recover from, but can detect. In a power-up generated initialization sequence, care must be given to the circuit that detects the event and generates the timed reset signal. The various power supply filters and loads must be considered as the state machine sequence should not be allowed to start until the entire power system is stable. Furthermore since some equipment and components may be damaged if they require multiple voltages that are not applied in the proper order, the computer control unit quite often is used to sequence the enabling of power supplies.

State "B" is the first computer minor cycle period. (A minor cycle is one primary clock period in length; characteristically, one microinstruction is executed. A major cycle is composed of one or more minor cycles and describes the completion of a macroinstruction or macroprocessors; i.e., "ADD" or "INTERRUPT"). During this state, the processor may be interrupted, halted, paused, or, in the absence of any of these requests, the computer control unit will fetch a macroinstruction from main memory and load it into the Instruction Register.

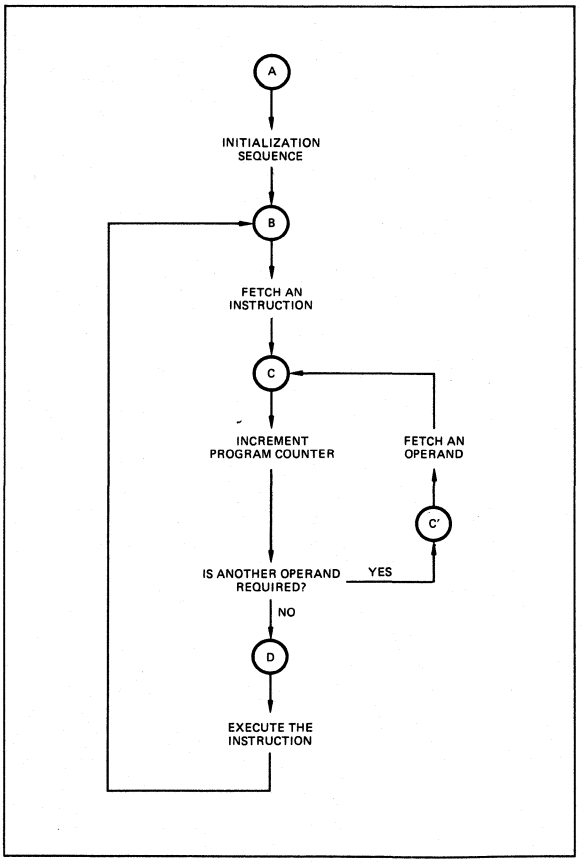


Figure 2. Simple Computer Control Unit State Transition Diagram.

Subsequently, during state "C", the Program Counter will be incremented and the instruction previously fetched will be decoded. If another operand is required for the current instruction, state "C" will be executed the necessary number of times, and the operands will be loaded into the appropriate registers until the requirements of the instruction have been satisfied.

The last state, "D", is where the macroinstruction is executed. As in all of the other states in the process, the instruction execution state may require one or more microinstruction cycles. Having completed this state, control of the CCU will revert to state "B" microcode after a microinstruction branch to the beginning of that sequence has been effected.

CCU ARCHITECTURE

A functional representation of a computer control unit is presented in Figure 3. To aid in the diagram reference process, the major subsystem components are labeled with the designations C_1 to C_8.

The Instruction Register, C_1, receives the instruction from main memory via the data bus. The width of the register is generally the same as the memory word and data bus width to conserve processor overhead time. That is, if one clock period is necessary to fetch an instruction and one clock period is used to execute the instruction, that is a much more efficient use of computer time than requiring two or more clock periods to fetch the instruction and only one clock period to execute it. Any time required by the processor over and above the instruction execution time is considered overhead.

An instruction is broken down into two or more fields: the "Op Code," and one or more operands. An Op Code (Operation Code) is the instruction itself. The operands are data used by the computer control unit in the execution of the instruction. For example, an operand might be the number of a selected register, a variable to be compared to the accumulator, the address of an input/output port, etc.

Because the operand may be used as data, it must be presented to the data bus via an open collector or three-state transmitter. The operand and its subfields must also be distributed to the other computer subsystems that is serves, such as, the register selectors in the arithmetic/logic unit. The decoding and use of the Op Code, however, is not as obvious conceptually or from an implementation standpoint.

There is usually more than one microinstruction per macroinstruction. And, different classes of macroinstructions almost always require a different number of microprogram steps. The designer that is interested in a computer with only a few instructions may eliminate some hardware by using the Op Code from the Instruction Register, C_1, directly as the starting address of the Microprogram ROM, C_4. This is not only

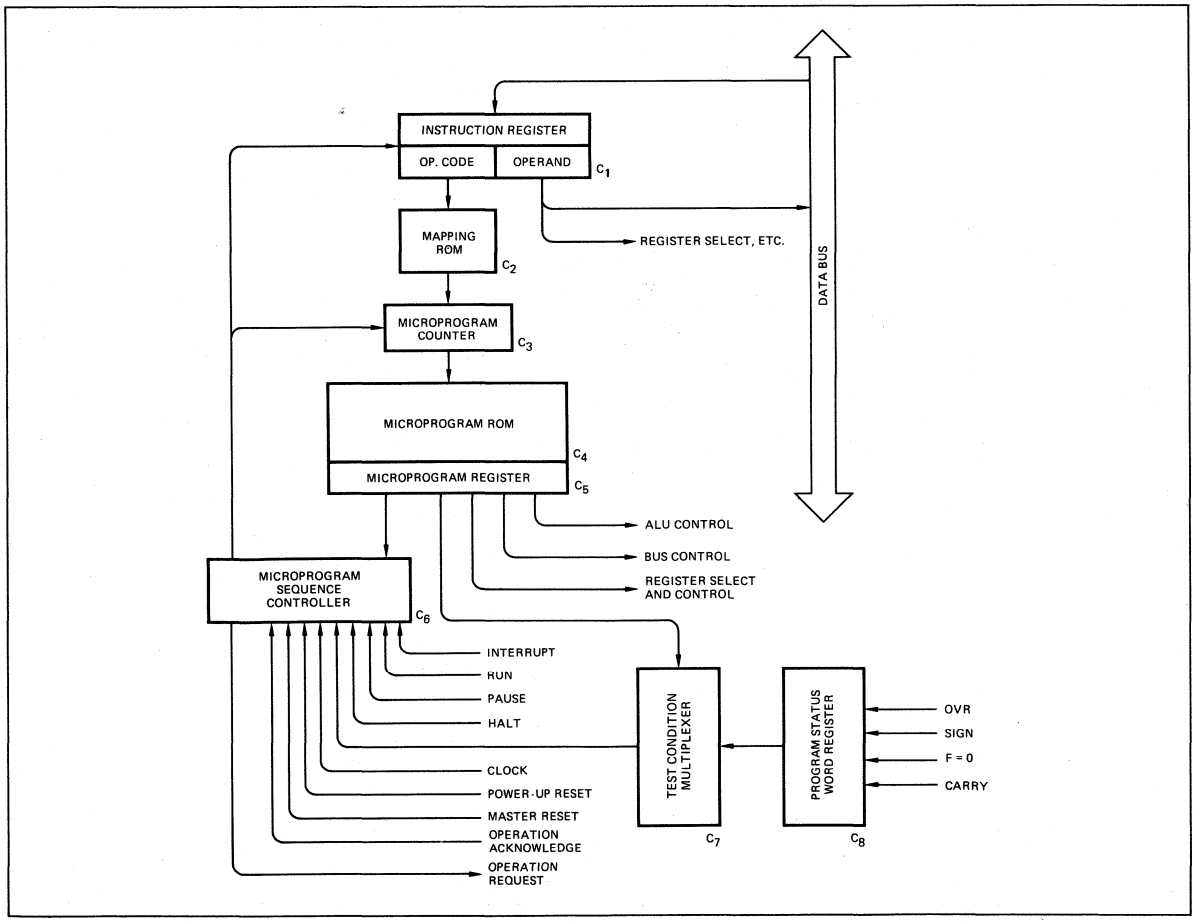


Figure 3. Computer Control Unit Architectural Schematic.

wasteful of Op Codes and inflexible, but, it means that any change in the instruction set or microprogram perturbs the entire system. To avoid this problem a Mapping ROM may be used.

The output of the Mapping ROM, C_2, should be wider than the Op Code field that is used as the address input. This allows a greater range of starting address for the Microprogram ROM, C_4. Because ROM/PROM field widths are typically 4 or 8-bits wide, a reasonable choice of width for the Mapping ROM with an 8-bit Op Code is 12-bits. The starting address is loaded into the Microprogram Counter, C_3, which points to the first microinstruction in the Microprogram ROM. When the output of the Microprogram ROM stabilizes, it is loaded into the Microprogram Register, C_5.

The use of the Microprogram Register in this manner is called pipelining. A pipeline register speeds up a state machine of this sort because it allows the address of the Microprogram ROM to be changed, and its output to settle, while the current microinstruction is being presented to the computer hardware from the Microprogram Register.

The Microprogram Sequence Controller, C_6, has two basic functions: it synchronizes events external to the CCU with the CCU, and it uses the output of the Test Condition Multiplexer to determine whether or not microprogram branches, jumps-to-subroutine, and returns-from-subroutine are to be made.

The external signals in the Microprogram Sequence Controller can be classified into five categories: supervisory, condition codes, initialization, synchronization, interrupts and clocks. Supervisory signals include "Run", "Halt", and "Pause". "Run" is a latched signal that enables the clock to the entire computer system. "Halt" disables the clock from the system, but it is only recognized during the instruction fetch microcycle; it too is latched. "Pause" is a level provided to the controller from an outside processor to temporarily suspend CCU control so that the external processor has uncontended access to the computer's resources. "Pause" is also only recognized during an instruction fetch microcycle.

Condition codes are stored in the Program Status Word Register, C_8, and presented to the Test Condition Multiplexer, C_7, where any of the codes may be selected by one of the microprogram fields in the microprogram register. If true, the output of the Test Condition Multiplexer will enable a branch instruction in the microprogram. The condition codes are loaded into the Program Status Word Register after every ALU operation or interrupt request.

Initialization lines include "Power-up Reset" and "Master Reset". The use of these lines was covered in some detail above.

The synchronization lines include "Operation Request" and "Operation Acknowledge", OPREQ and OPACK. These signals allow external events that may be slower than the CCU to be synchronized to the CCU. For example, when the CCU issues a memory reference instruction, an OPREQ is also generated, and, although the system clock continues to run, it is disabled from the CCU. When the addressed memory bank has achieved its access time and performed the read or write operation, it must generate an OPACK which will be synchronized with the system clock which will in turn enable the clock to the CCU. When the memory or I/O cycle times are known and can be controlled, the CCU clock period can be adjusted to preclude the requirement for synchronizing signals.

An interrupt may occur at any time, however, it is only recognized at an instruction fetch microcycle. At the time the interrupt is allowed, the priority encoded interrupt vector is jammed into the Program Status Word Register and the Microprogram ROM address is forced to the interrupt service routine address. When the interrupt has been serviced, the Microprogram Counter is returned to instruction fetch minor cycle address and processing resumes.

CCU INSTRUCTIONS

As implied earlier, there are two types of instructions recognized within the CCU, machine language or macroinstructions, and random logic replacement or microinstructions. Macroinstructions reside in main memory, are fetched and loaded into the instruction register and then decoded into microinstructions which directly control the computer's resources.

An example of two different types of macroinstructions may be seen in Figure 4a. A 16-bit instruction was defined with a constant length Op Code defined in the least significant 8 bits of the instruction. The remainder of the instruction word, bits 8 through 15, will be defined as a function of instruction type.

The register-to-register instruction has two operand fields that select the source and destination register, Register A and Register B, respectively. That is, the result of an arithmetic/logic function with Registers A and B will be sotred in Register B.

The branch instruction's operand is an 8-bit displacement address. With the condition of the branch implicit in the Op Code, the sum of the current Program Counter address and the displacement address will be stored in the program counter if the selected condition is logically true.

A microinstruction word format is depicted in Figure 4b. Four bits, b_{0-3}, are used to define the type of microinstruction being executed. The second field of 4-bits, b_{4-7}, selects the branch condition if the microinstruction is a branch instruction, enables the interrupt and pause functions if the microinctruction is a macroinstruction fetch command and disables the interrupts at all other times. The third microinstruction field is composed of two 3-bit subfields which are used to define the source and the destination of data on the data bus. The remaining 12-bit field is defined either as an arithmetic logic unit control field or as a microprogram branch address field depending on the microinstruction function. Although there are a number of methods for mapping various types of microinstruction control fields into a microinstruction, this straightforward approach will be followed, for the purpose of an implementation example and only one mapped field function will be assumed: ALU control and branch address.

CCU IMPLEMENTATION USING Am2909

As an example, the computer control unit arthitectural schematic of Figure 3 will be reduced to practice to aid in the illustration of the Am2909 Microprogram Sequencer. The Am2909 is an extremely valuable subsystem component in that it allows the designer to take advantage of the latest microprogramming techniques; microbranching, microsubroutines and repetitive microinstruction execution. Also, because of the architecture of the component itself, the CCU is inherently faster than a classical implementation of the same function. That is, the classical design may use sequential circuits which must be parallel loaded and sequentially incremented with separate clock pulses, while the Am2909 uses a combinational incrementor outside of the microprogram address bus which is transferred to the microprogram counter

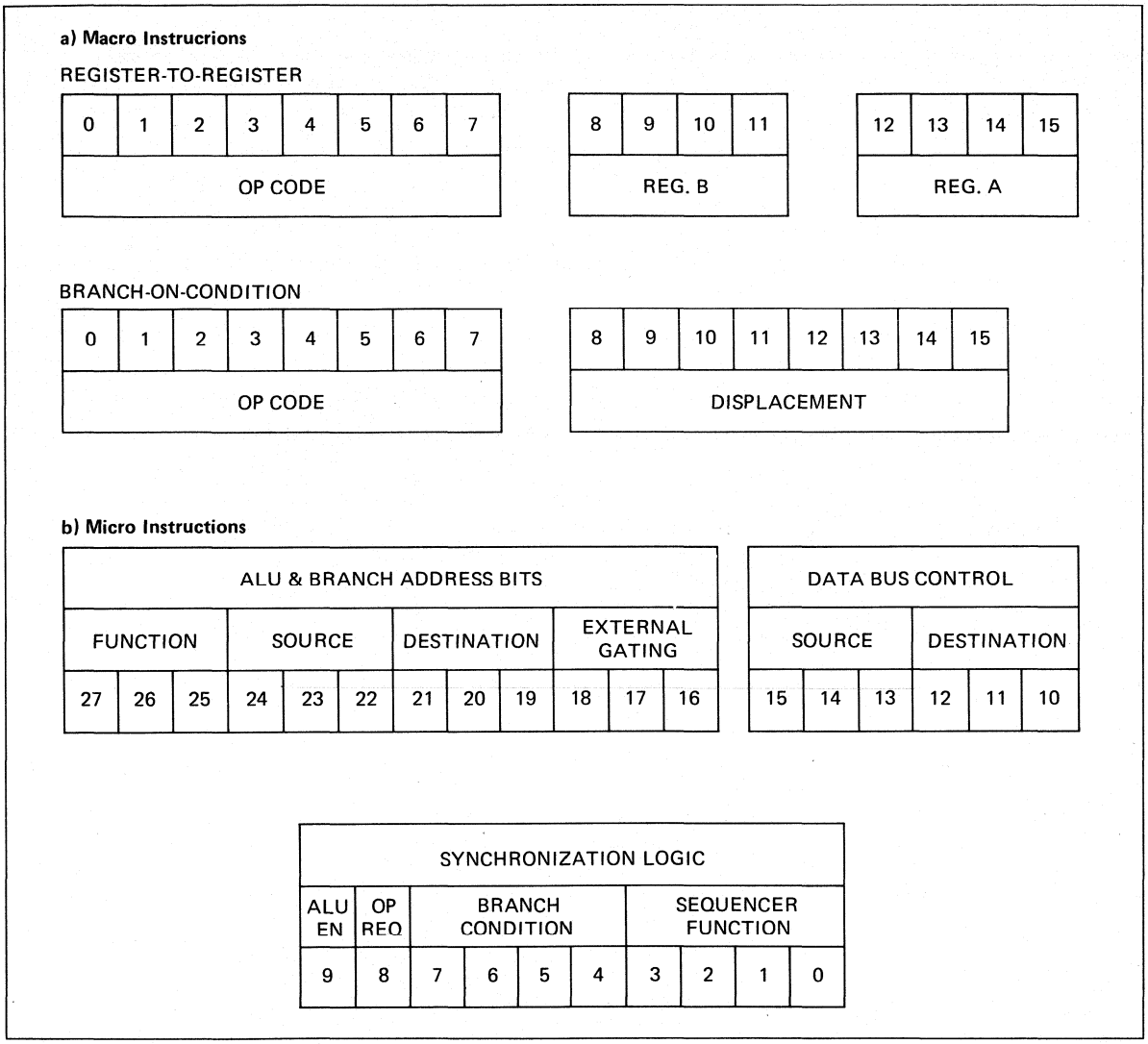


Figure 4. Example Macro and Micro-Instruction Fields.

on the rising edge of the clock pulse. A detailed specification of the Am2909 is provided in the expanded data sheet and its internal architectural rendering is reproduced here in Figure 5.

The purpose of the Am2909 is to present an address to the microprogram ROM such that a microinstruction may be fetched and executed. In referencing Figure 5, there are four sources of address information available: an Address Register, a Microprogram Counter Register, a Direct or branch input, and a subroutine stack. The address source is chosen by using the one-of-four address multiplexer select lines, S_0 and S_1. The selected address may then be modified by the OR input lines or the $\overline{ZERO}$ input function before it is presented at the Y address output lines through a three-state buffer.

The OR input lines may be used in one of two manners. Selected OR inputs may be placed at logic "1" which will provide the logical OR of the selected address source and the OR input lines at the Y output. This allows the address to be "masked". If a microprogram instruction of the Skip or Branch classes is being executed and the microinstruction is aligned on an even address microprogram ROM word (the least significant address bit is "0"), then the least significant OR input may be controlled by an external test condition multiplexer. If the result of the conditional test was logically false, then the least significant bit may be modified to avoid the execution of the Branch or Skip instruction. All of the unused inputs must be tied to ground. Similarly, if the 2, 3, 4, or n-least significant bits of the selected address are "0", the associated OR input lines may be modified for an extended address range skip capability.

Sometimes, in a state machine like a computer control unit, it is desirable to easily get to a predefined state, or address. For instance, if the machine has just been turned on and it is necessary to perform an initialization sequence or a real-time event occurs where the processor control is required but the on-going process information may not be destroyed, such as

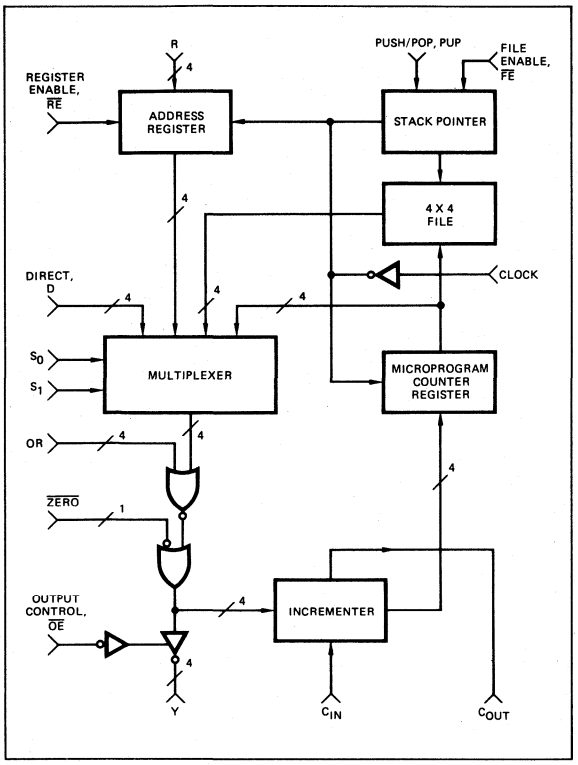


Figure 5. Am2909 Microprogram Sequencer Architecture.

an interrupt, the OR inputs may be used. All of the OR inputs must be connected to the output of a positive logic gate so that when the event occurs the output of the gate goes to logical "1", as does the Y output address lines. $\overline{ZERO}$ provides a similar capability, but it must normally be held at logic "1" and only "pulled down" to "0" when the event occurs – causing all of the address output lines to go to "0"

The three-state output buffer that drives the Y-lines may be used nicely to allow automatic test of the memory and register system. That is, if the buffer output control, $\overline{OE}$, is disabled, the Y-lines go into a high impedance condition allowing the automatic tester's output lines to be connected directly across the outputs. This capability also allows multiple processors to share the same memory by enabling only one processor's Y-bus at a time.

The Address Register, as well as all other storage devices on the Am2909, is parallel loaded from the R inputs when the register enable line, $\overline{RE}$, is low on a positive going clock transition. This is a good register to use when entering the starting address of a microprogram. If selected, the contents of the register are not only presented to the Y outputs, but also to the Incrementer.

The Incrementer is a full-adder provided with an off-chip carry-in signal, C_{IN}, and a off-chip carry-out signal, C_{OUT}, allowing multiple Am2909's to be cascaded. The output from the Incrementer is connected to a parallel load input on the Microprogram Counter Register where it is loaded on the rising edge of the next clock pulse. If the Microprogram Counter is selected as the source address by subsequent microinstructions, it will be incremented by each succeeding clock pulse, thereby stepping through the microprogram.

As described above, it is often valuable to provide a branch instruction and a branch address in a microprogram instruction. The data lines from the branch address field in the microinstruction may be feedback to the Direct, D, input on the Am2909. The source address multiplexer may then select the branch input as the next microinstruction address. This address will be incremented and stored in the Microprogram Counter Register on the next clock pulse which provides the address for the following instruction.

The push/pop, or last-in, first-out stack, allows the microprogrammer to have the same subroutine execution flexibility that machine language programmers have. Heretofore a luxury in almost all computers microsubroutines may be nested four deep. There is a 4-bit wide by 4-word file whose address is controlled by a 2-bit up/down counter. A push/pop control signal, PUP, determines whether the function being performed is a jump-to-subroutine, PUSH, or a return-from-subroutine, POP. When the File Enable control line, $\overline{FE}$, is low, the push/pop command will be executed on the next clock pulse rising edge. After the subroutine has been completed, a return to the address immediately following the jump-to-subroutine instruction may be accomplished by selecting the stack as the source address and executing a POP at the same time.

An example implementation of the computer control unit of Figure 3 using the macro and microinstruction form of Figure 4 is depicted in Figure 6. A 16-bit data bus and memory word were assumed as reflected by the Instruction Register. Four Am2918 4-bit, TTL/three-state output registers, U_{1-4}, are used for the Instruction Register. The two least significant registers, U_1, and U_2, contain the Op Code, while U_3 and U_4 contain the Operand field. The TTL output from the Op Code register pair is not used, but rather the three-state outputs are connected to the address input of the macroinsctruction Mapping PROM. If the output enable, $\overline{OE}$, of the pair is held low by pulling up the input of an inverter, as shown, then the trouble-shooting and automatic testing of the subsystem will be much more simple. In this way, the tester can gain control over the memory system. The three-state output buffers for the Operand field are fed back to the eight least significant bits of the data bus so that they may be used to modify the contents of some other register in the system. For ALU functions, the Operand field will most likely be used as two 4-bit subfields to specify a source register, R_A, and a source/destination register, R_B. (In fact, this arrangement works extremely well if the Am2901 Microprocessor is employed.) The TTL outputs are used for R_A and R_B data.

The mapping PROM's that were used, selected for their speed and architecture, are three Am29761's in parallel. With a memory configuration of 256 words by 4 bits, each of the 256 potential Op Codes has a unique 12-bit starting address which provides the designer with a lot of flexibility for his initial design and an unusually easy task of adding more instructions at a later date.

In turn, the Mapping PROM outputs are connected to the address register inputs, R_{0-11}, of the three Am2909 Microprogram Sequencers. The Microprogram Sequencer outputs, Y_{0-11}, provide the address inputs for seven Am29761 Microprogram PROM's. (The output enable lines of the Am2909's should be controlled in the same manner as the Instruction Register outputs.) Although only 256 words of microprogram storage are shown, up to 4096 words may be implemented if necessary. Furthermore, if more than 28-bit microinstruction words are required for the user's task they may be added as necessary.

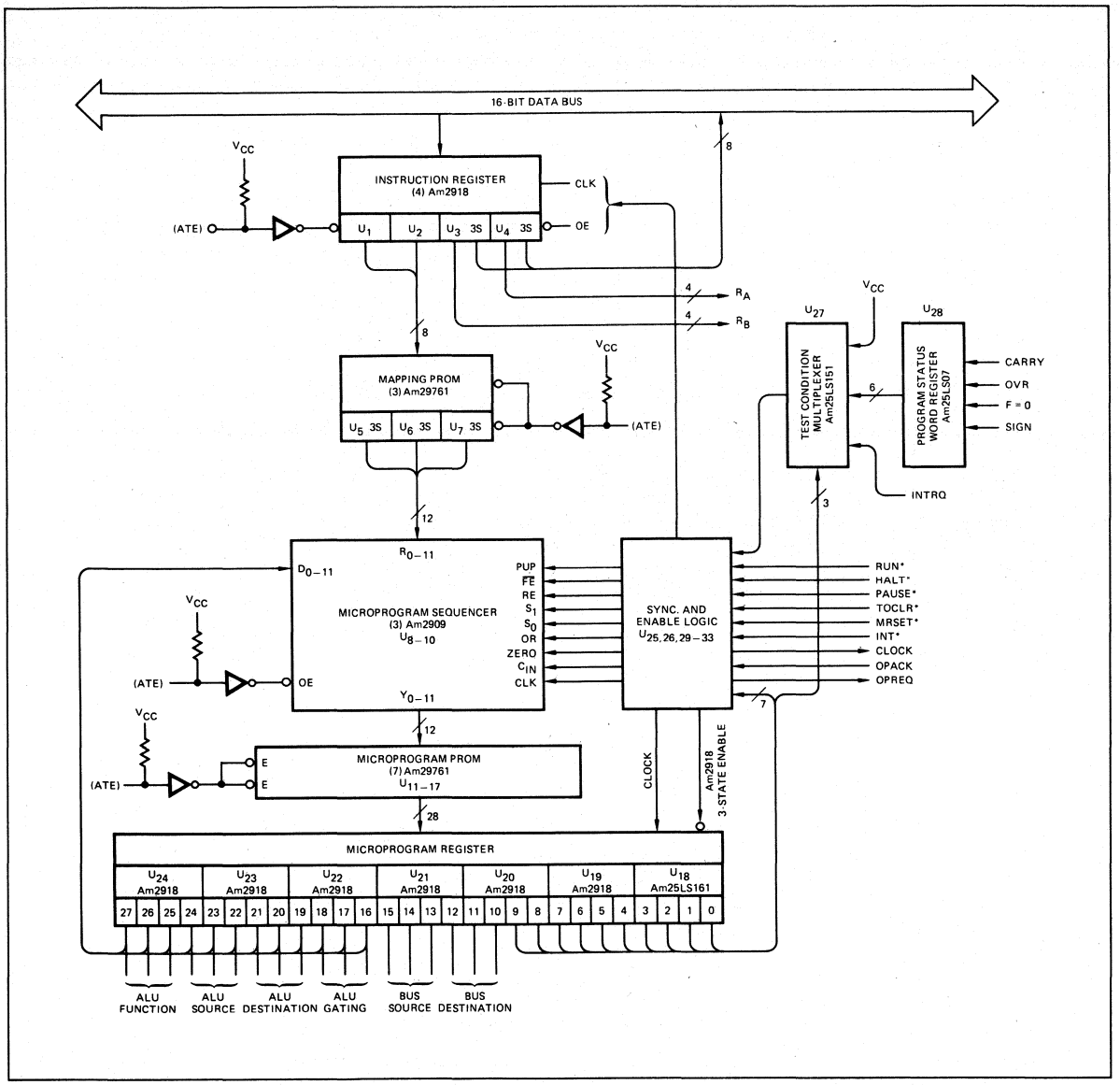


Figure 6.

The Microprogram Register consists of one Am25LS161 register, U_{18}, and six Am2918 registers, U_{19-24}. The ten least significant bits are used by the synchronization and enable logic. The most significant 12 bits are used for either Microsequencer branch address (the TTL outputs of the Am2918's) or for control of the ALU (the 3-state lines are used). In this configuration, the starting address from the mapping PROM is loaded into the sequencer's internal register at some time prior to its being needed. An alternative configuration is to connect the mapping PROM to the Direct inputs, allowing a branch to the starting address on one cycle. If the D inputs are used for the mapping PROM, the microsequencer branch address can be loaded from the microprogram PROM outputs into the sequencer's register. In this case, the internal register serves as a duplicate microprogram register. A third choice is to connect the mapping PROM outputs and the microprogram register outputs together onto a three-state bus which drives the sequencer's direct inputs. Either the mapping PROM or Branch address is enabled onto the bus at the appropriate time.

As shown, the ALU control bit fields are specified to control four Am2901's and perform all of the necessary external gating and bit manipulation. The remaining six central bits are provided for data bus source and destination controls and the 3-state outputs are used. Whenever the processor is running the 3-state output enable lines are held low, enabling the output. If the processor has been Paused, austensibly for direct memory access, the outputs are disabled so that an external or peripheral processor can gain access to the control line.

The Sync. and Enable Logic is relatively complex and may be shown better in Figure 7. The two least significant registers in the Microprogram registers, U_{18} and U_{19}, are at the top of the page. In addition, the remaining 2 bits from the Microprogram Register that are used here, ALUEN* and OPREQ, are shown with rectangular boxes around them so that they are easy to see. The control and status bits that eminate from portions of the computer other than the CCU are shown enclosed in ovals. All other signals are generated or used with the CCU.

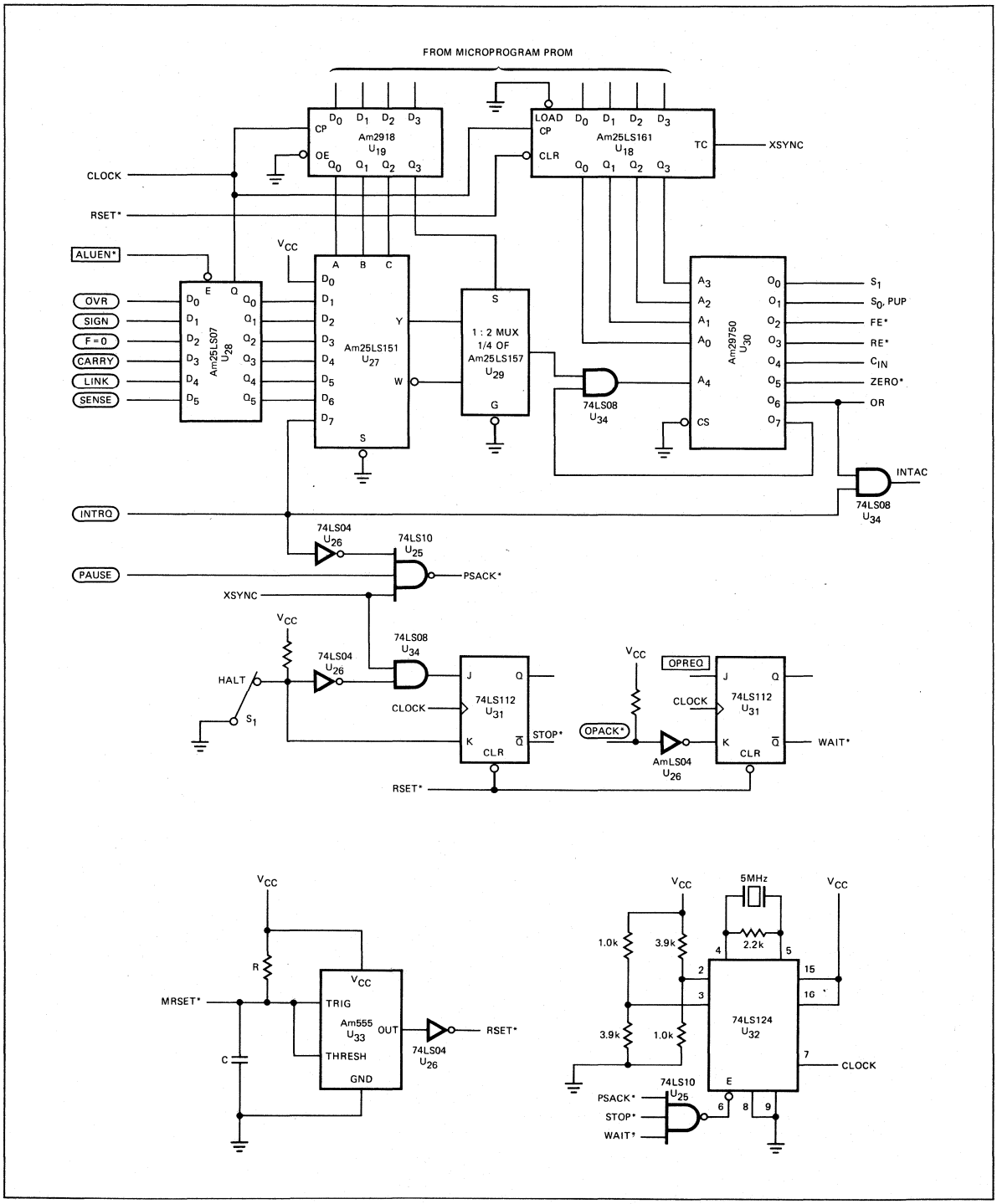


Figure 7. Sync. and Enable Logic Diagram.

The 4 bits stored in Microprogram Register U_{18} provide the Microprogram Sequencer Function instruction. An Am25LS161 was selected for this register because it was synchronous, has an asynchronous clear (enabling power-up reset) and is low-power Schottky. These 4 bits provide the least significant address bits of an Am29750 32-word by 8-bit PROM, as well as providing an external event synchronizing signal enable, XSYNC. With XSYNC at logic "1", the external processes that use PAUSE will be enabled allowing direct memory access.

The Am29750 PROM has eight open collector outputs (that must have pull-up resistors added). Seven of the output signals go directly to the 3 sets of Am2909 control lines. The eighth output line is fed back to enable a gate that drives the fifth PROM address line. The other signal at the AND-gate, U_{34}, is the test condition enable line.

The test condition signal is the result of selecting one of eight processor condition signals using the Am25LS151 multiplexer, U_{27}. U_{27} has two outputs, the selected signal and its complement. One of these two signals is selected using (1/2) Am25LS157, U_{29}, as the multiplexer. The 4-bit select signal is stored in Microprogram Register U_{19}. Notice that one of the condition code multiplexer's inputs is tied to V_{CC} which provides for an unconditional branch if the entire register, U_{19}, is "0". Six of the condition codes (from the ALU) are stored in an Am25LS07 register. Everytime an ALU function is selected and clocked, as denoted by ALUEN*, the current value of the condition codes are clocked into U_{28}. The eighth condition code bit is the interrupt request signal INTRQ which is latched externally.

Before proceeding with the rest of the synchronization and enable circuitry, let us consider the programmability aspects of this portion of the state machine. A table of desirable Microprogram Sequencer functions is provided in Figure 8. In fact, this table is also the memory map for the Microprogram Sequencer PROM, U_{30}. Entries are made in the table by U_{30} address value. The first 16 entries have the test condition address bit equal to "0". These are the primary instructions; they enable the Am2909 functions. Of the primary instructions there are only four that have O_7, the test condition enable bit set. Three of these are branch instructions and for these microinstructions any condition code may be specified in register U_{20} except interrupt request, INTRQ. The remaining instruction relates to the macroinstruction fetch process (Figure 2) and only during this microcycle may be CCU be interrupted or paused, as data or instructions moved to system registers under microprogram control may be lost if the microprocess is disturbed. Processed interrupts, by definition, disturb the microprocess and may usurp control of any of the computer's resources.

The only instance when there will be a secondary instruction defined, is when bit O_7, equals "1" such that potentially A_4 equals "1". In the event that the condition code test was successful, the four secondary instructions defined in Figure 8 will be executed.

If an interrupt was generated during an instruction fetch, the OR output, U_{30}, O_6, will assume logic "1". This signal will be logically ANDed by U_{34} to generate the interrupt acknowledge signal, INTAC. INTRQ, or the absence of the granting of the external synchronization signal, XSYNC, that is generated during the instruction fetch, will preclude the pause acknowledge signal, PSACK*.

An attempt to Halt the processor using an external switch S_1 will also be denied unless the current microinstruction cycle is a macroinstruction fetch. Starting the processor by moving switch S_1 to the RUN position will always be granted and synchronized by U_{31} because by definition the processor stopped previously at an instruction fetch cycle which is also the first state which must be executed when the processor is turned on. If STOP, the Q output of U_{31} is logic "0", the processor will HALT.

Provision has been made to synchronize the relatively fast CCU with relatively slow memory or input/output functions. If a microinstruction causes memory or I/O reference, the microprogrammer must set the OPREQ bit true. This signal is latched-up in the second half of flip-flop U_{31} and stops the processor (WAIT = "0") until the address device acknowledges the operation is complete or the data is ready by pulling down the OPACK* line. U_{31} synchronizes the event and restarts the processor.

We have discussed a "hard" processor interrupt event, INTRQ, a "soft" interrupt (one where the state of the processor is not disturbed, but operation is suspended), PAUSE, starting and stopping the processor, RUN and HALT, and synchronizing the processor with external events, OPREQ/OPACK*. Let us consider the system clock and system initialization.

A good choice for a system oscillator is the 74LS124, U_{32}. This device is a dual voltage controlled oscillator whose timing may be derived either by a series mode, fundamental frequency crystal, or an RC timing circuit. For high speed digital circuits, it is necessary to use a crystal. The output of the oscillator is free running and is presented to an on-chip pulse synchronizer controlled by the enable line on the chip. No partial pulses can be passed by the synchronizer so that control of the oscillator's enable line may be asynchronous. A PAUSE, HALT, or OPREQ will cause the gated oscillator to shut off until the process is allowed to restart.

Initialization of a state machine is very important. When the power is applied to the system, the system must be disabled until all of the power supply filters have charged and the regulators stabilized. Also, critical storage devices must be preset to a known state. To accomplish this, an Am555 timer circuit, U_{33} with output buffer, U_{26}, is used. The RC value should yield a time-out circuit increment greater than 100msec in most systems (t = 1.1RC for this device). Also, by using an external switch or open collector gate to ground a MRSET*, the entire system may be master reset without cycling the power supply off and then on again. Other than clearing flip-flops, the output of the initialization circuit RSET*, clears the Microprogram Register U_{18}. By referring to Figure 8 again, it can be seen that Microsequencer Function $A_{0\text{-}3}$ = "0" provides system initiation in that U_{30} output bit O_5, ZERO*, is low, thereby setting the initial microprogram address to zero and incrementing from there. This allows an initialization microprogram to be stored in the bottom of memory.

The ability to execute the same microinstruction a number of times was alluded to previously. Generally the value of this capability lies outside of the CCU. As an example, let us reconsider the macroinstruction format for a Register-to-Register instruction (Figure 4). If the Op Code is a Shift or Rotate instruction, it would be desirable to allow the programmer to move the data word over a range of 1 to 16-bit positions with a single instruction rather than having to execute the same instruction many times. Since there are two Operand subfields, R_A and R_B, let us define the 4-bit value in R_A as the number of bit positions we wish to move the

	MICROPROGRAM SEQUENCER FUNCTION					FUNCTION DESCRIPTION	MICROPROGRAM SEQUENCER CONTROL							
							O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
	A_4	A_3	A_2	A_1	A_0		TEST ENABLE	OR	$\overline{ZERO}$	C_{IN}	$\overline{RE}$	$\overline{FE}$	S_0, PUP	S_1
TEST CONDITION DISABLED OR FALSE	0	0	0	0	0	Initialize System	L	X	L	H	H	H	X	X
	0	0	0	0	1	Branch Test	H	L	H	H	H	H	L	L
	0	0	0	1	0	Jump to Subroutine Test	H	L	H	H	H	H	L	L
	0	0	0	1	1	Return from Subroutine	H	L	H	H	H	H	L	L
	0	0	1	0	0	Execute Program	L	L	H	H	H	H	L	L
	0	0	1	0	1	External Carry Control	L	L	H	*	H	H	L	L
	0	0	1	1	0		L	L	H	H	H	H	L	L
	0	0	1	1	1		L	L	H	H	H	H	L	L
	0	1	0	0	0		L	L	H	H	H	H	L	L
	0	1	0	0	1	This Group Undefined	L	L	H	H	H	H	L	L
	0	1	0	1	0		L	L	H	H	H	H	L	L
	0	1	0	1	1		L	L	H	H	H	H	L	L
	0	1	1	0	0		L	L	H	H	H	H	L	L
	0	1	1	0	1		L	L	H	H	H	H	L	L
	0	1	1	1	0	Load Mapped (Starting) Address	L	L	H	H	L	H	H	L
	0	1	1	1	1	Fetch Instruction	H	L	H	H	H	H	L	L
TEST CONDITION ENABLED AND TRUE	1	0	0	0	0	This State Undefined	L	–	–	–	–	–	–	–
	1	0	0	0	1	Execute Branch	H	L	H	H	H	H	H	H
	1	0	0	1	0	Execute Jump	H	L	H	H	H	L	H	H
	1	0	0	1	1	Execute Return	H	L	H	H	H	L	L	H
	1	0	1	0	0		L	–	–	–	–	–	–	–
	1	0	1	0	1		L	–	–	–	–	–	–	–
	1	0	1	1	0		L	–	–	–	–	–	–	–
	1	0	1	1	1		L	–	–	–	–	–	–	–
	1	1	0	0	0		L	–	–	–	–	–	–	–
	1	1	0	0	1	This State Undefined	L	–	–	–	–	–	–	–
	1	1	0	1	0		L	–	–	–	–	–	–	–
	1	1	0	1	1		L	–	–	–	–	–	–	–
	1	1	1	0	0		L	–	–	–	–	–	–	–
	1	1	1	0	1		L	–	–	–	–	–	–	–
	1	1	1	1	0		L	–	–	–	–	–	–	–
	1	1	1	1	1	Service Interrupt or Pause	H	H	H	H	H	H	X	X

*Value of this Bit depends on Logic Implementation. See Text.

Figure 8. Microsequencer Function Table.

data, and R_B as the general purpose register that will be effected. (The additional hardware to implement the circuit is shown in Figure 9.)

The value in R_A must be parallel loaded into a 4-bit binary counter that has a terminal count flag, TC (when $Q_0 = Q_1 = Q_2 = Q_3 = 1$, TC = 1), such as the Am25LS163. The Am2909 control signal RE*, that loads the Address Register, must also be applied to the Am25LS163 signal LOAD*. CLOCK is merely the system clock, and MLTEN is a signal that must be supplied by the microprogram to enable this function. MLTEN and TC are connected to an open-collector AND-gate which pulls down the Am2909 carry-in line until terminal count has been achieved. As a result, the microprogram address does not change until TC equals "1" and then C_{IN} equals "1" which increments the microprogram counter causing the next instruction to be executed. The number of reasons for using this feature are almost unlimited, as are the means to implement the function.

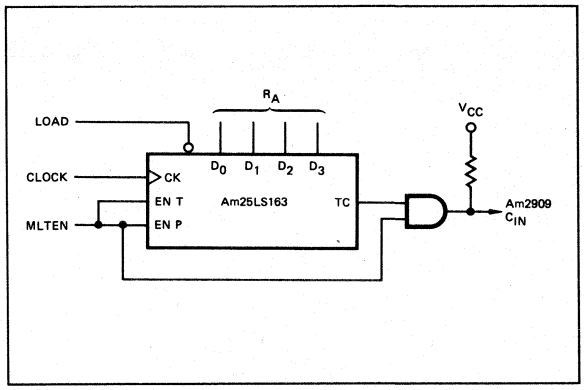


Figure 9. Iterative Microinstruction Control Circuit Example.

Am2913

Priority Interrupt Expander

Distinctive Characteristics

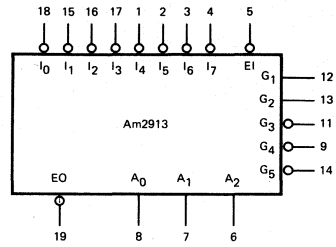
- Encodes eight lines to three-line binary
- Expands use of Am2914
- Cascadable
- Similar in function to Am54LS/74LS/25LS148
- Gated three-state output
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

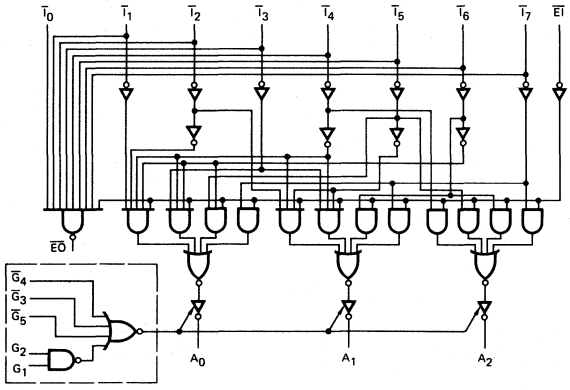
The Low-Power Schottky Priority Interrupt Expander is an extention of the Am2900 series of Bipolar Processor family and is used to expand and prioritize the output of the Am2914 Priority Interrupt circuit. Affording an increase of vectored priority interrupt in groups of eight, this unit accepts active LOW inputs and produces a three-state active HIGH output prioritized from active I_7 to I_0. The output is gated by five control signals, three active LOW and two active HIGH. Also provided is a cascade input (EI) and Enable Output (EO).

One Am2913 will accept and encode group signal lines from up to 8 Am2914's (64 levels of interrupt). Additional Am2913's may be used to encode more interrupt levels.

LOGIC SYMBOL



LOGIC DIAGRAM



TRUTH TABLE

Inputs									Outputs			
$\overline{EI}$	$\overline{I_0}$	$\overline{I_1}$	$\overline{I_2}$	$\overline{I_3}$	$\overline{I_4}$	$\overline{I_5}$	$\overline{I_6}$	$\overline{I_7}$	A_0	A_1	$\overline{A_2}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G1 = H, G2 = H, G3 = L, G4 = L, G5 = L

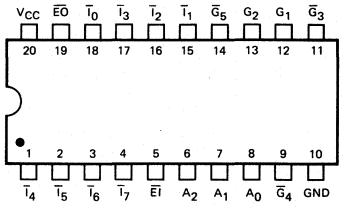
G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

Z = HIGH Impedance

ORDERING INFORMATION

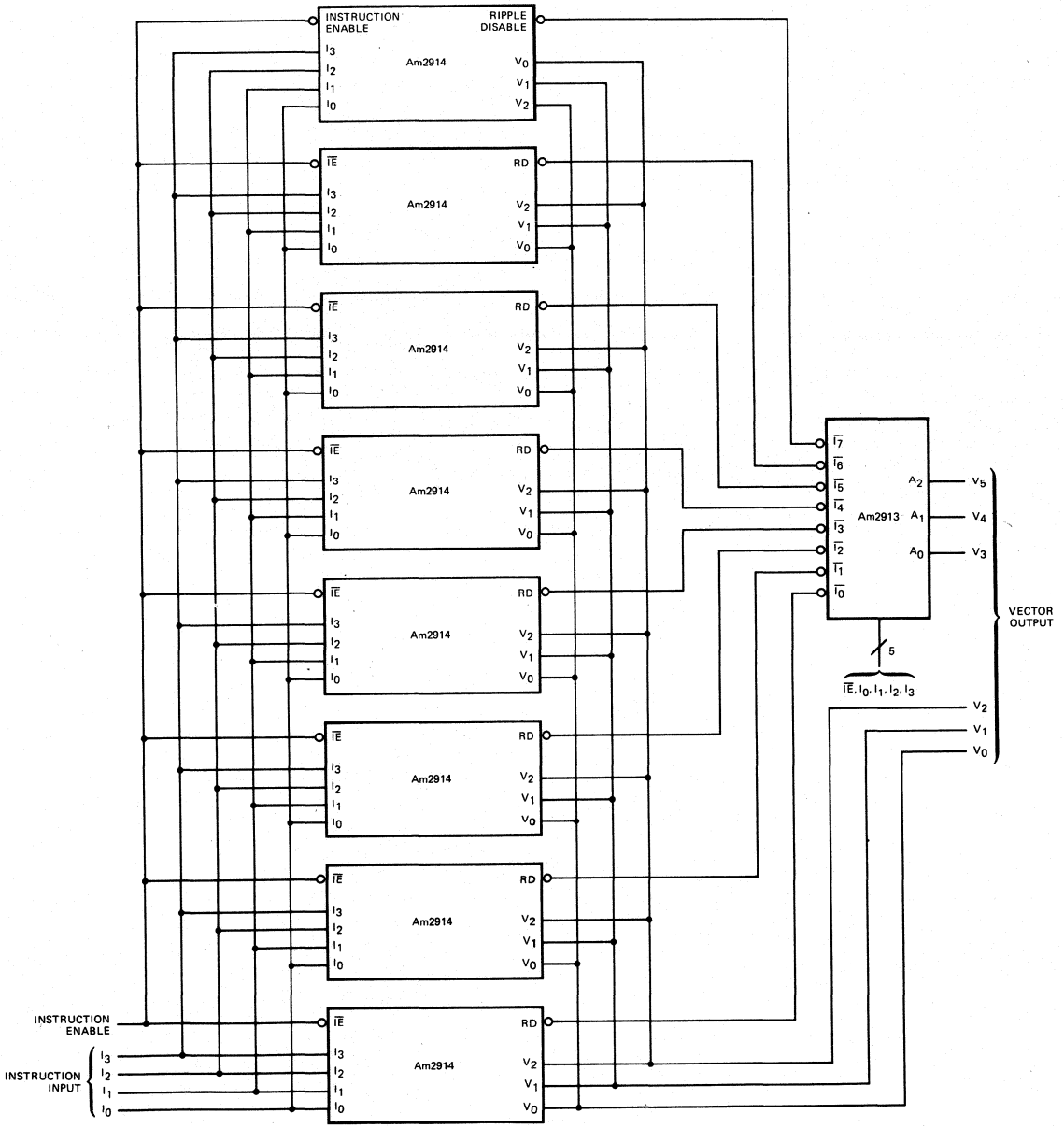
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2913PC
Hermetic DIP	0°C to +70°C	AM2913DC
Dice	0°C to +70°C	AM2913XC
Hermetic DIP	–55°C to +125°C	AM2913DM
Hermetic Flat Pak	–55°C to +125°C	AM2913FM
Dice	–55°C to +125°C	AM2913XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

APPLICATION



Shown above is the connection of the instruction lines and vector output lines in a 64-input priority interrupt system. The Am2913 is used to encode the most significant bits associated with the vector output.

Am2914

Vectored Priority Interrupt Encoder

DISTINCTIVE CHARACTERISTICS

- Accepts 8 interrupt inputs
  Interrupts may be pulses or levels and are stored internally
- Built-in mask register
  Six different operations can be performed on mask register
- Built-in status register
  Status register holds code for lowest allowed interrupt
- Vectored output
  Output is binary code for highest priority un-masked interrupt
- Expandable
  Any number of Am2914's may be stacked for large interrupt systems
- Microprogrammable
  Executes 16 different microinstructions
  Instruction enable pin aids in vertical microprogramming
- High-speed operation
  Delay from an interrupt clocked into the interrupt register to interrupt request output is typically 70ns

FUNCTIONAL DESCRIPTION

The Am2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The high-speed of the Am2914 makes it ideal for use in Am2900 family microcomputer designs, but it can also be used with the Am9080A MOS microprocessor.

The Am2914 receives interrupt requests on 8 interrupt input lines (P_0-P_7). A LOW level is a request. An internal latch may be used to catch pulses on these lines, or the latch may be bypassed so the request lines drive the edge-triggered interrupt register directly. An 8-bit mask register is used to mask individual interrupts. Considerable flexibility is provided for controlling the mask register. Requests in the interrupt register are ANDed with the corresponding bits in the mask register and the results are sent to an 8-input priority encoder, which produces a three bit encoded vector representing the highest numbered input which is not masked.

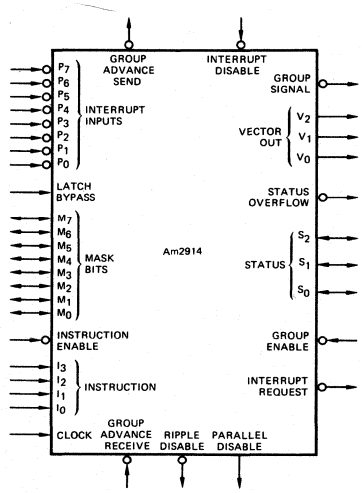
An internal status register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the status register are compared with the output of the priority encoder, and an interrupt request output will occur if the vector is greater than or equal to status. Whenever a vector is read from the Am2914 the status register is automatically updated to point to one level higher than the vector read. (The status register can be loaded externally or read out at any time using the S pins.) Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A status overflow output indicates that an interrupt has been read at the highest priority.

The Am2914 is controlled by a 4-bit instruction field I_0-I_3. The command on the instruction lines is executed if IE is LOW and is ignored if IE is HIGH, allowing the 4 I bits to be shared with other devices.

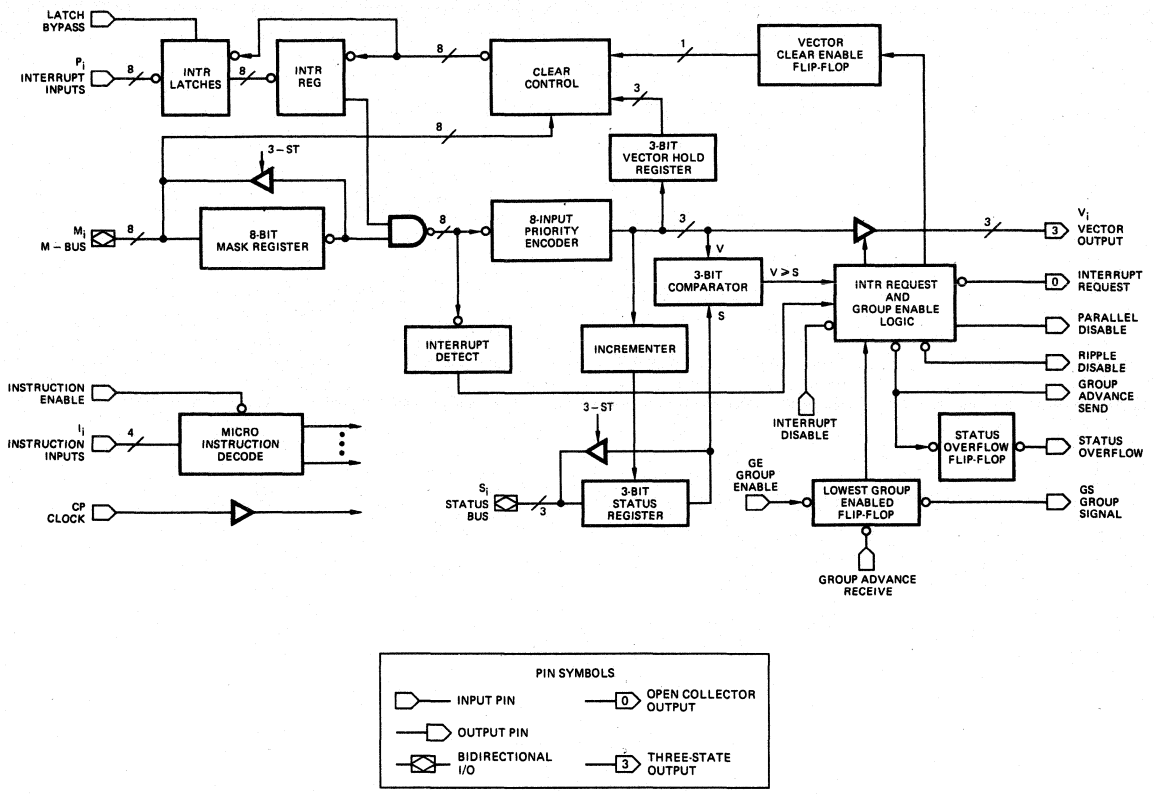
ORDERING INFORMATION

Package Type	Temperature Range	Part Number
Molded DIP	0°C to +70°C	AM2914PC
Hermetic DIP	0°C to +70°C	AM2914DC
Dice	0°C to +70°C	AM2914XC
Hermetic DIP	–55°C to +125°C	AM2914DM
Hermetic Flat Pak	–55°C to +125°C	AM2914FM
Dice	–55°C to +125°C	AM2914XM

LOGIC SYMBOL



BLOCK DIAGRAM



BLOCK DIAGRAM DESCRIPTION

The Microinstruction Decode circuitry decodes the Interrupt Microinstructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal.

The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector is used for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S Bus. During a Vector Read, the Incrementer increments the interrupt vector by one, and the result is clocked into the Status Register. Thus the Status Register always points to the lowest level at which an interrupt will be accepted.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of 2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

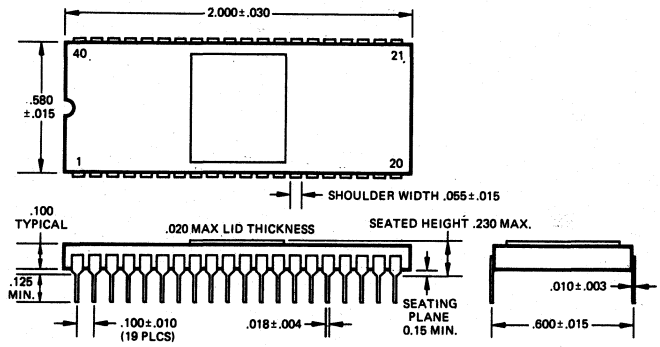
The Status Overflow signal is used to disable all interrupts. It indicates the highest priority interrupt vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this group. When it is set, it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

PHYSICAL DIMENSIONS

40-Pin Ceramic (Side Brazed)



$\theta_{JC} \approx 20°C/W$
(MIL-STD-883, Method 1012C2)

TABLE I

MICROINSTRUCTION SET FOR Am2914 PRIORITY INTERRUPT CIRCUIT

Decimal
$I_3I_2I_1I_0$

Mask Register Functions

14 Load mask register from M bus
7 Read mask register to M bus
12 Clear mask register (enables all priorities)
8 Set mask register (inhibits all interrupts)
10 Bit clear mask register from M bus
11 Bit set mask register from M bus

Status Register Functions

9 Load status register from S bus and LGE flip-flop from GE input
6 Read status register to S bus

Interrupt Request Control

15 Enable interrupt request
13 Disable interrupt request

Decimal
$I_3I_2I_1I_0$

Vectored Output

5 Read vector output to V outputs, load V+1 into status register, load V into vector hold register and set vector clear enable flip-flop.

Priority Interrupt Register Clear

1 Clear all interrupts
3 Clear interrupts from mask register data (uses the M bus)
2 Clear interrupts from M bus data
4 Clear the individual interrupt associated with the last vector read

Master Clear

0 Clear all interrupts, clear mask register, clear status register, clear LGE flip-flop, enable interrupt request

STANDARD SCREENING

(Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Level	
			Am2914PC, DC	Am2914DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C 24-hour 150°C	100%	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B 10,000 G	100% *	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/cm^3	100% *	100%
Gross Leak	1014	C2 Fluorocarbon	100% *	100%
Electrical Test Subgroups 1 and 7	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 7
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 7

*Not applicable for Am2914PC.

ADDITIONAL SCREENING FOR CLASS B PARTS

Step	MIL-STD-883 Method	Conditions	Level
			Am2914DMB, FMB
Burn-In	1015	D 125°C 160 hours min.	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

GROUP A SUBGROUPS

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum Rated Temeperature
11	Switching	Minimum Rated Temperature

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	+0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

P/N	Ambient Temperature	V_{CC}
Am2914PC, DC	0°C to +70°C	4.75V to 5.25V
Am2914DM, FM	−55°C to +125°C	4.50V to 5.50V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2914XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2914XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA	2.4			Volts
			COM'L, I_{OH} = −2.6mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	Interrupt disable			−1.44	mA
			Instruction enable			−1.08	
			Others			−0.72	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	Interrupt disable			80	μA
			Instruction enable			60	
			Others			40	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	Interrupt disable			0.2	mA
			Instruction enable			0.2	
			Others			0.2	
I_{OZ}	Output OFF Current	V_{CC} = MAX.	V_{OUT} = 0.4V			−20	μA
			V_{OUT} = 2.7V			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.					mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

APPLICATIONS

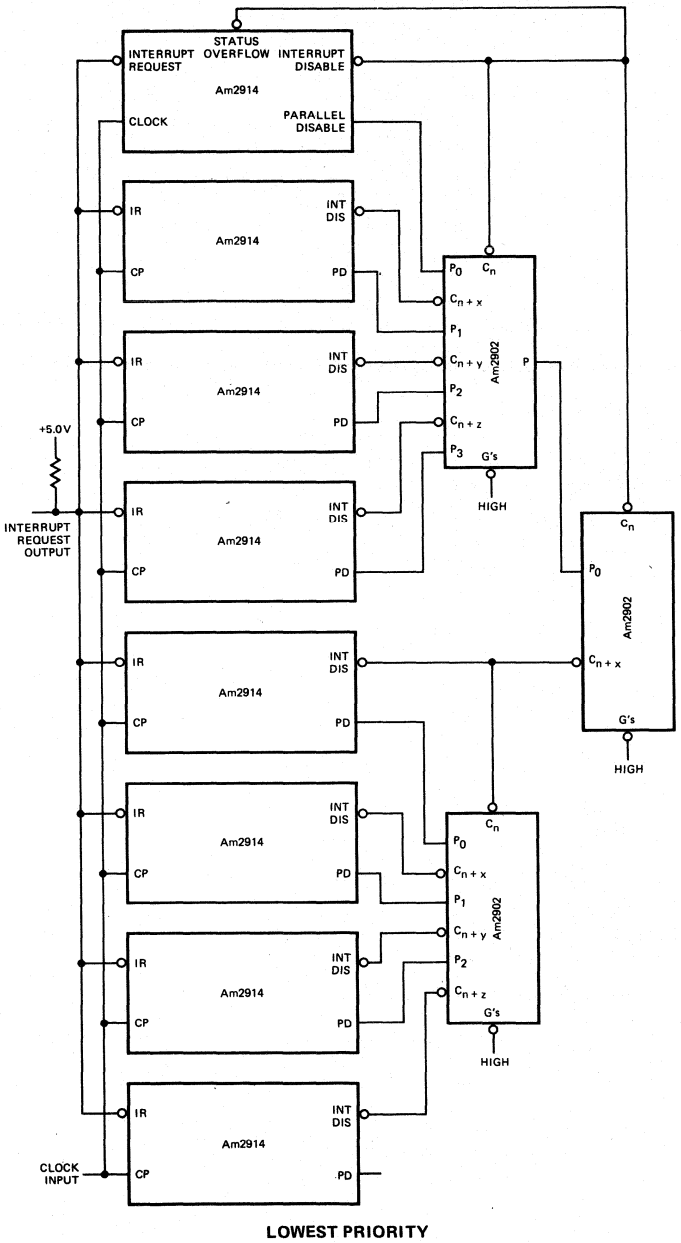


Figure 1.

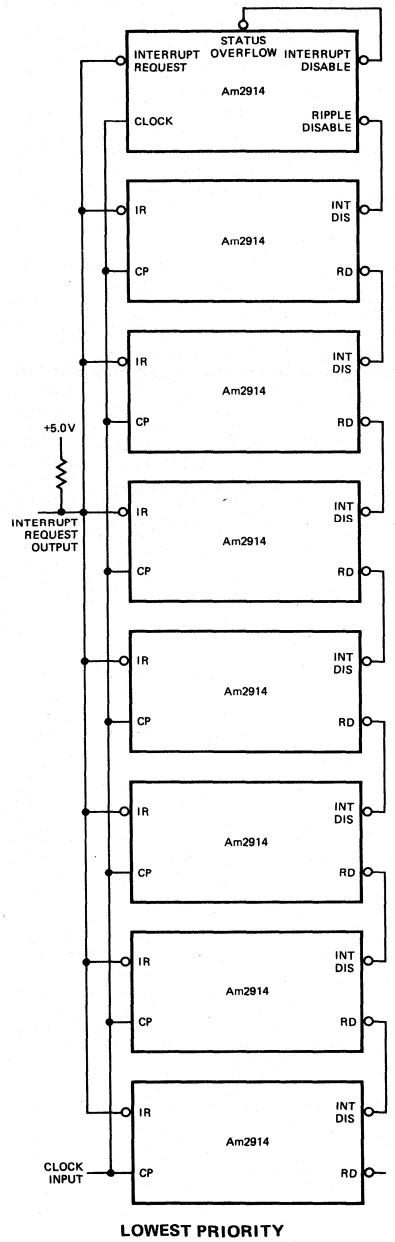


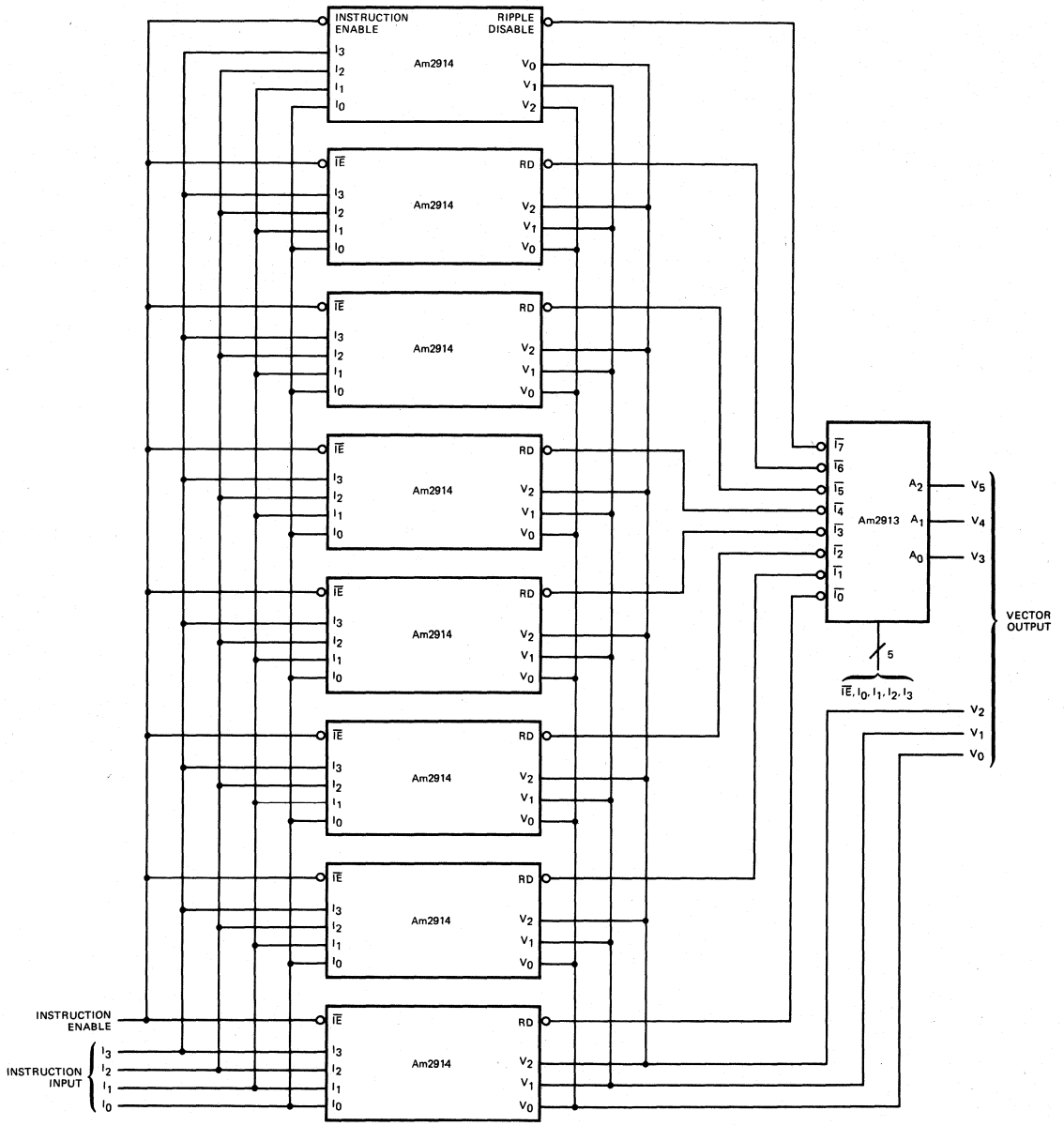
Figure 2.

Figures 1, 3 and 4 show the connections required for a high-speed, parallel disable of lower priority interrupts.

This connection scheme for a 64-input priority interrupt system uses three Am2902's for high-speed disable of lower prioritites.

Figures 2, 3 and 4 show the connections required for a ripple disable of lower priority interrupts. For a ripple disable scheme, the Ripple Disable pin of each group is connected to the Interrupt Disable pin of the next lower priority group.

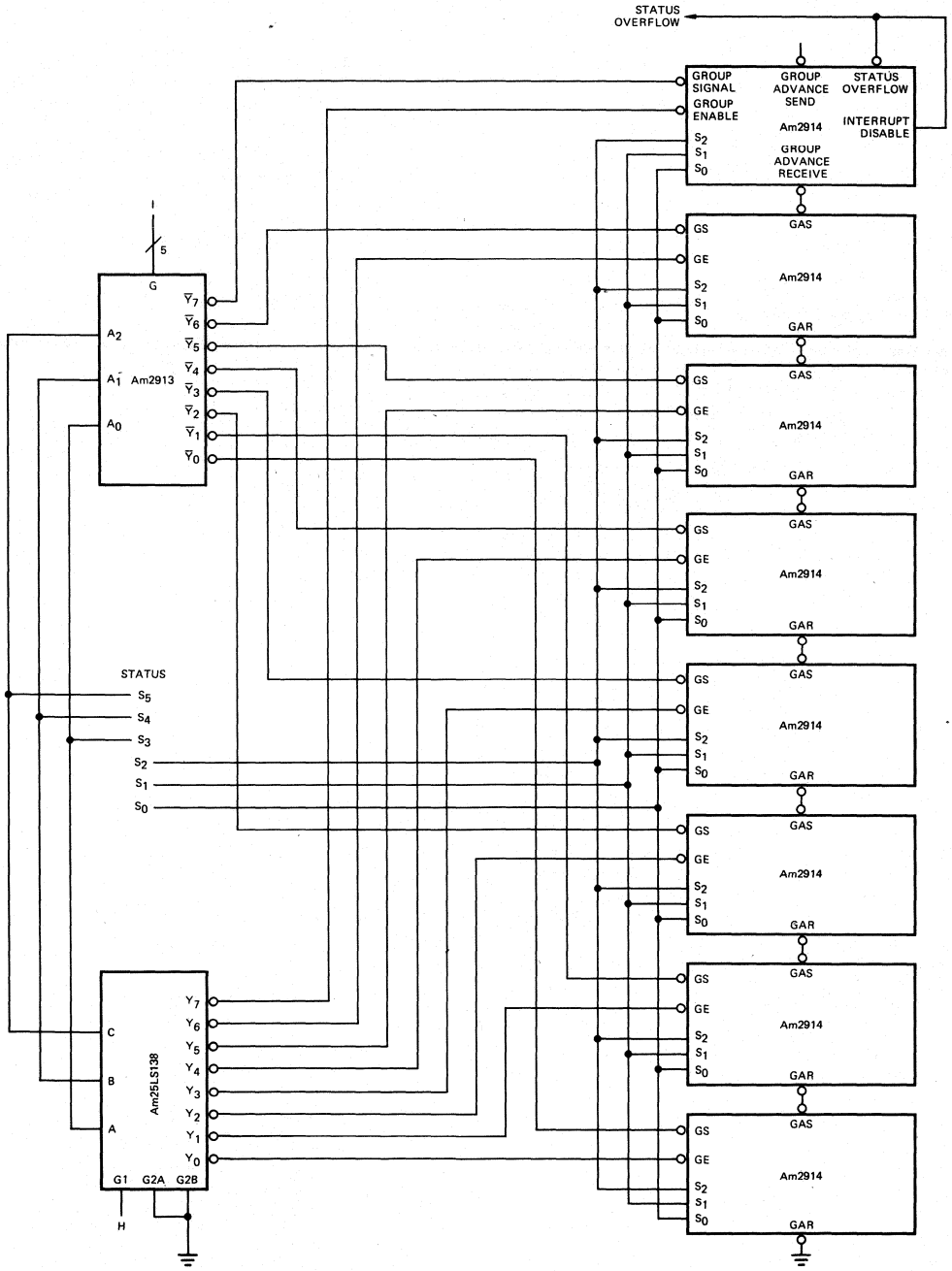
APPLICATIONS (Cont.)



Shown above is the connection of the instruction lines and vector output lines in a 64-input priority interrupt system. The Am2913 is used to encode the most significant bits associated with the vector output.

Figure 3.

APPLICATIONS (Cont.)



Connection of the status inputs and group enable control in a 64-input priority interrupt system.

Figure 4.

Am2915

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 40mA at 0.5V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2915 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and Low-Power Schottky inputs.

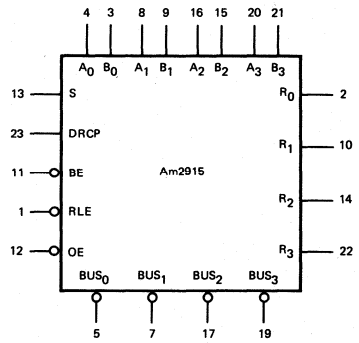
The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and OE LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

ORDERING INFORMATION

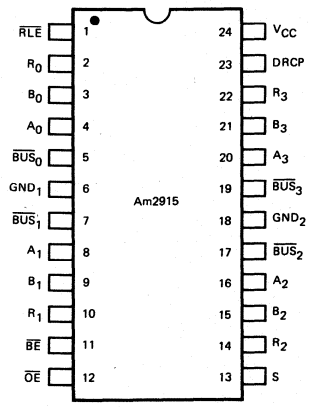
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2915PC
Hermetic DIP	0°C to +70°C	AM2915DC
Dice	0°C to +70°C	AM2915XC
Hermetic DIP	−55°C to +125°C	AM2915DM
Hermetic Flat Pak	−55°C to +125°C	AM2915FM
Dice	−55°C to +125°C	AM2915XM

LOGIC SYMBOL

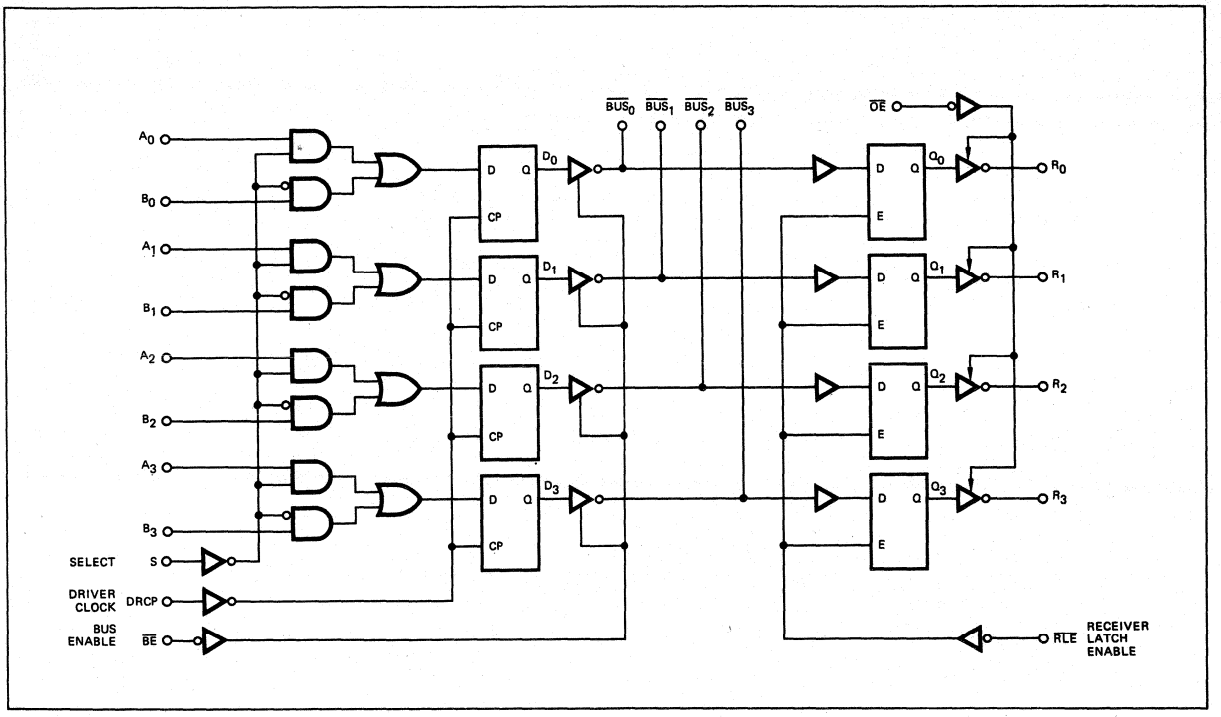


V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915XC(COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V

Am2915XM(MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 40mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	I_{OH} = −20mA	2.4			Volts
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V				0.8	Volts
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0V		−50	−85	−130	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915XC(COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2915XM(MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		$V_{CC} = 5.0$V, $I_{OH} = -100\mu$A		3.5			
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4.0$mA		0.27	0.4	Volts
			$I_{OL} = 8.0$mA		0.32	0.45	
			$I_{OL} = 12$mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4$V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 7.0$V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			60	90	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	$V_O = 2.4$V			20	μA
			$V_O = 0.4$V			−20	

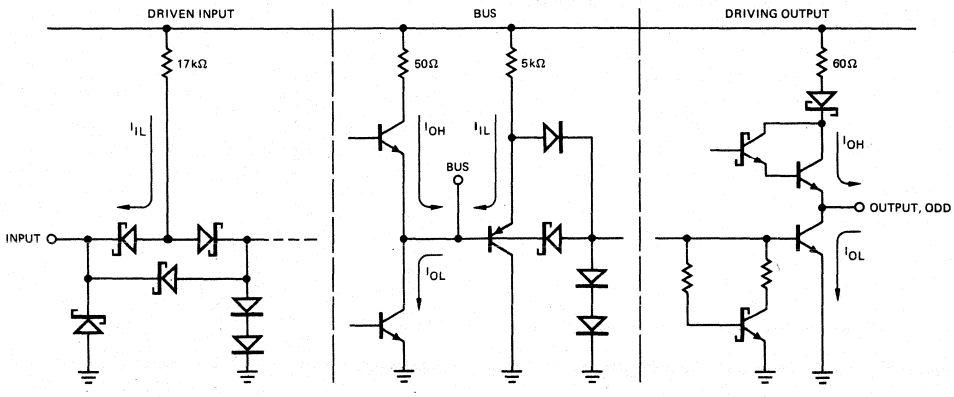
SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2915XM Min.	Am2915XM Typ. (Note 2)	Am2915XM Max.	Am2915XC Min.	Am2915XC Typ. (Note 2)	Am2915XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	26		13	23	
t_s	Data Inputs (A or B)		23			20			ns
t_h			8.0			6.0			
t_s	Select Input (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)	C_L = 15pF, R_L = 2.0kΩ		18	30		18	27	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	30		21	27	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		17			14			ns
t_h			6.0			4.0			
t_{ZH}, t_{ZL}	Output Control to Receiver Output			14	26		14	23	ns
t_{HZ}, t_{LZ}				14	26		14	23	

PRELIMINARY
THESE SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

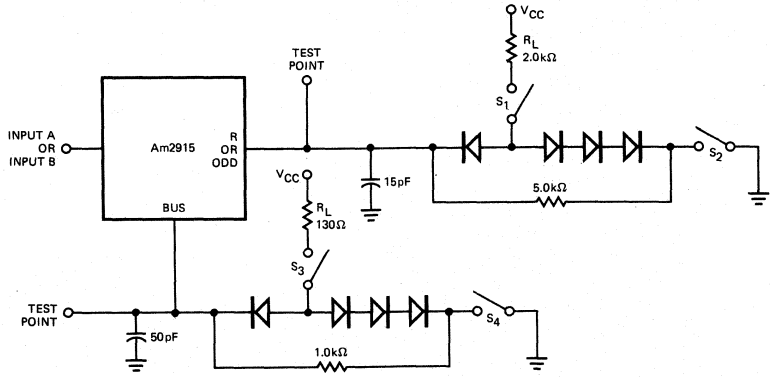
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

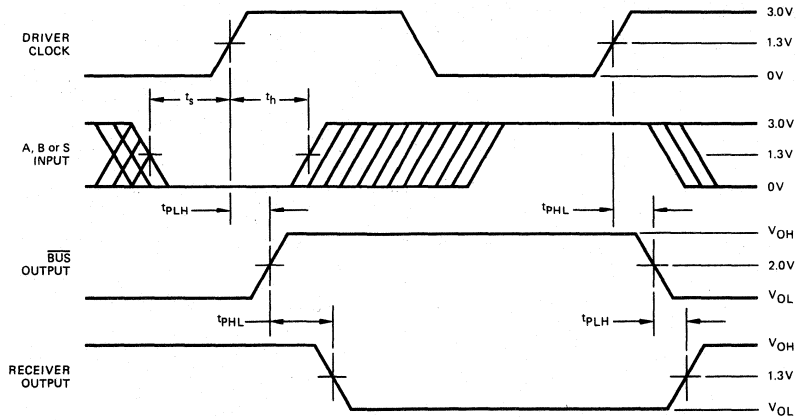


Note: Actual current flow direction shown.

SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS



Note: Bus to Reciver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

FUNCTIONAL TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

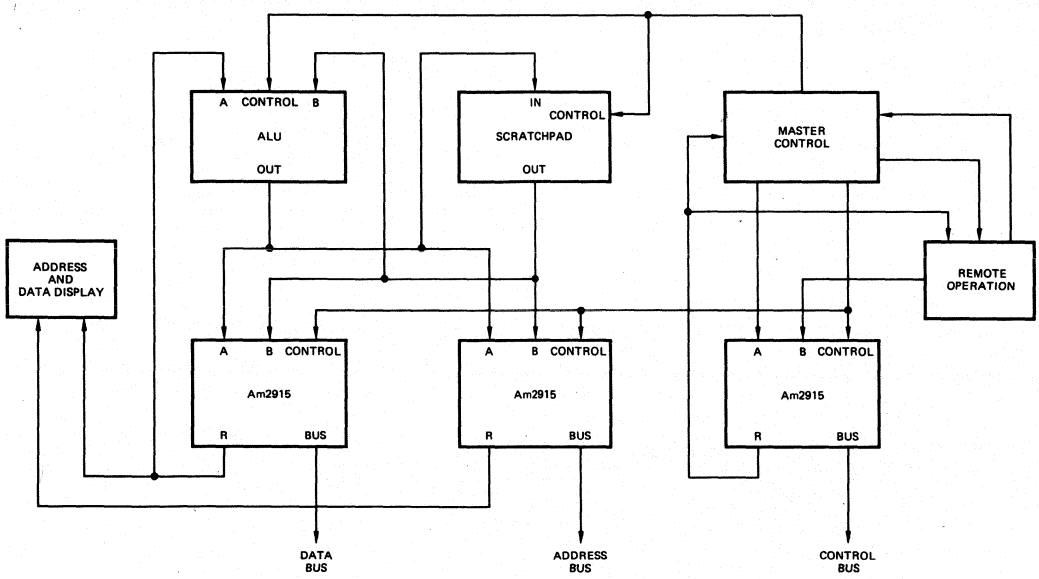
$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

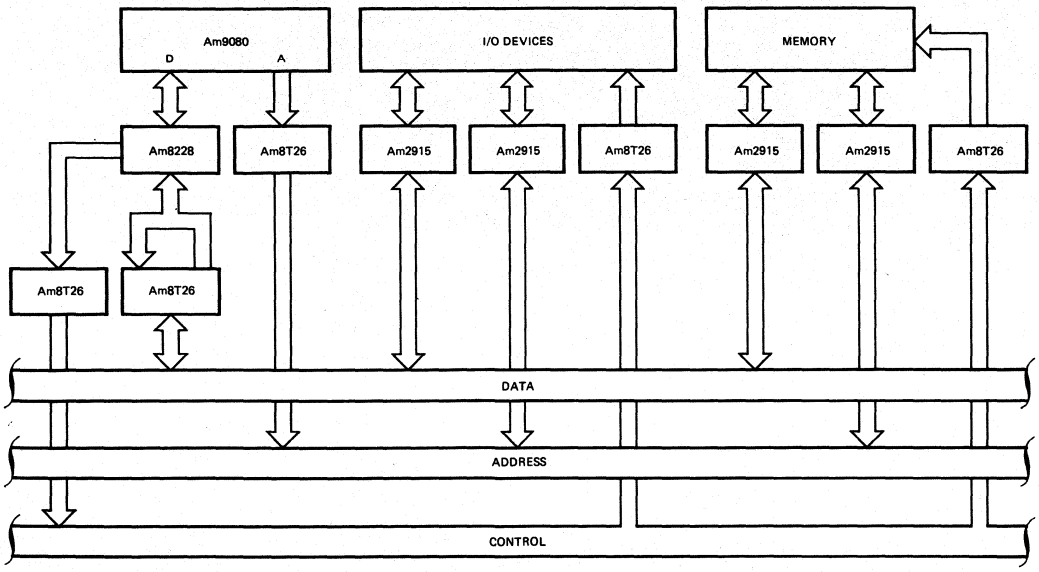
$\overline{RLE}$ Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

APPLICATIONS



The Am2915 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.



Using the Am2915 and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

Am2916

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 40mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2916 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

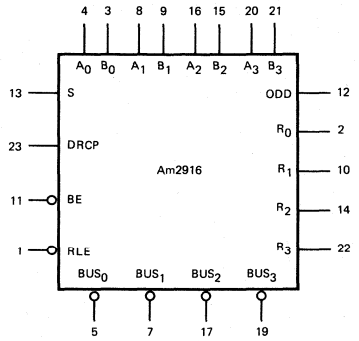
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

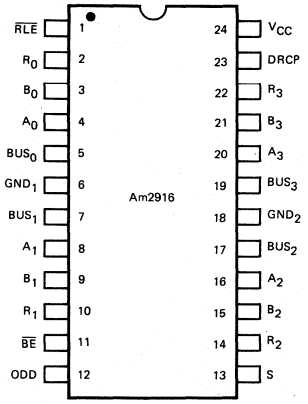
The Am2916 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

CONNECTION DIAGRAM
Top View

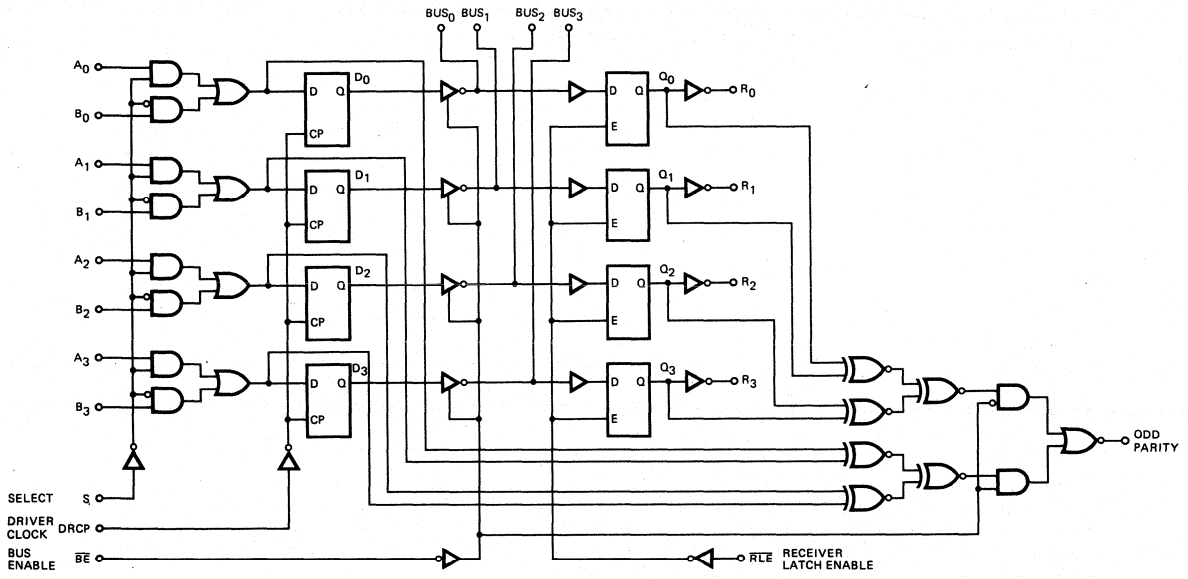


Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2916PC
Hermetic DIP	0°C to +70°C	AM2916DC
Dice	0°C to +70°C	AM2916XC
Hermetic DIP	−55°C to +125°C	AM2916DM
Hermetic Flat Pak	−55°C to +125°C	AM2916FM
Dice	−55°C to +125°C	AM2916XM

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916XC(COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V

Am2916XM(MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 40mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	I_{OH} = −20mA	2.4			Volts
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V, V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V				0.8	Volts
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX., V_O = 0V		−50	−85	−130	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916XC(COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V

Am2916XM(MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		V_{CC} = 5.0 V, $I_{OH} = -100\mu$A		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu$A, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND			75	110	mA

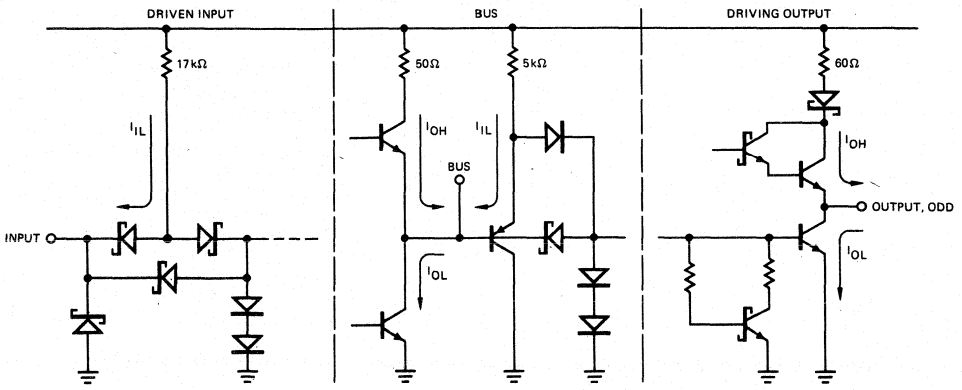
SWITCHING CHARACTERISTICS

Parameters	Description	Test Conditions	Am2916XM Min.	Am2916XM Typ. (Note 2)	Am2916XM Max.	Am2916XC Min.	Am2916XC Typ. (Note 2)	Am2916XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	26		13	23	
t_s	Data Inputs (A or B)		23			20			ns
t_h			8.0			6.0			
t_s	Select Inputs (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	30		18	27	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	30		21	27	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)	C_L = 15pF, R_L = 2.0kΩ	17			14			ns
t_h			6.0			4.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	

PRELIMINARY
THESE SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

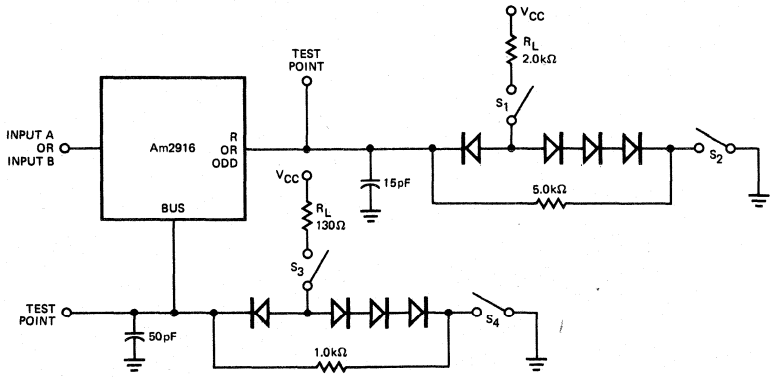
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test shoul not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

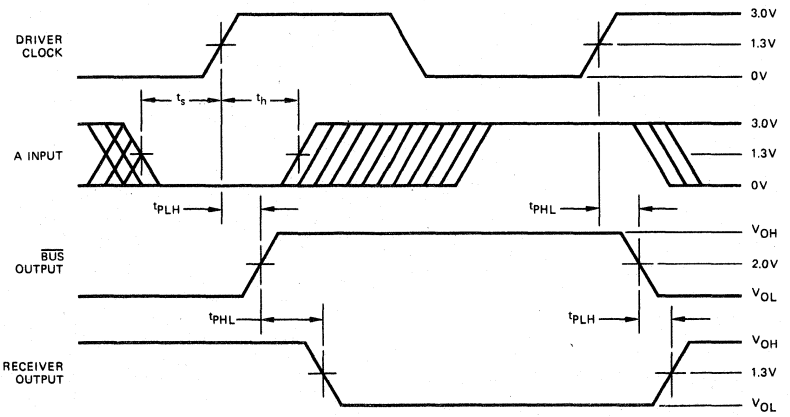


Note: Actual current flow direction shown.

SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW-to-HIGH transition

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

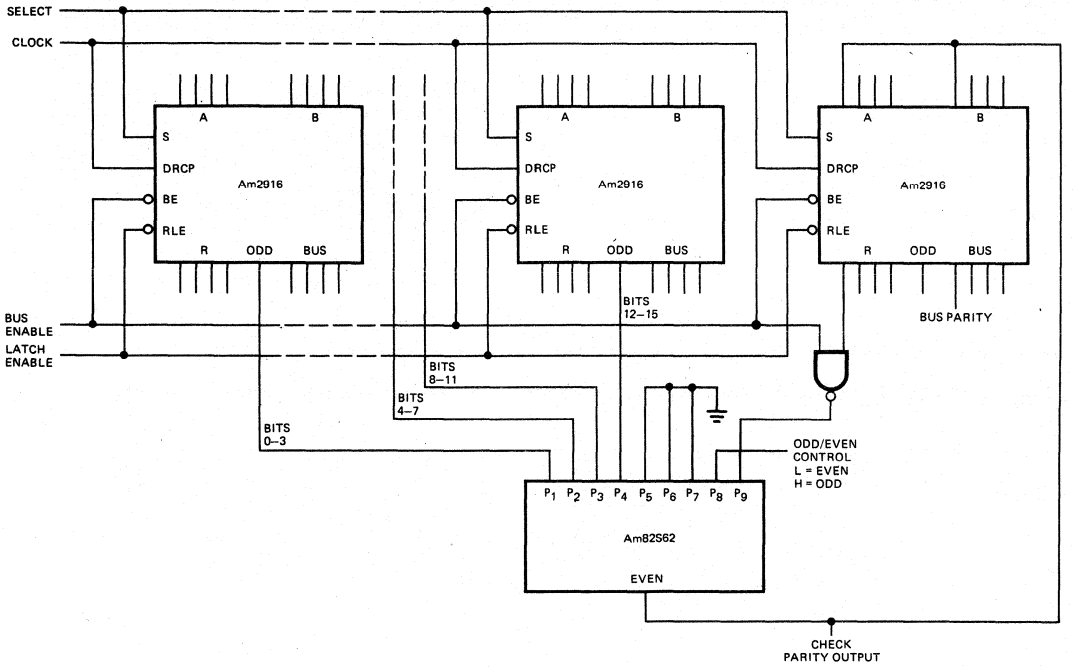
$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

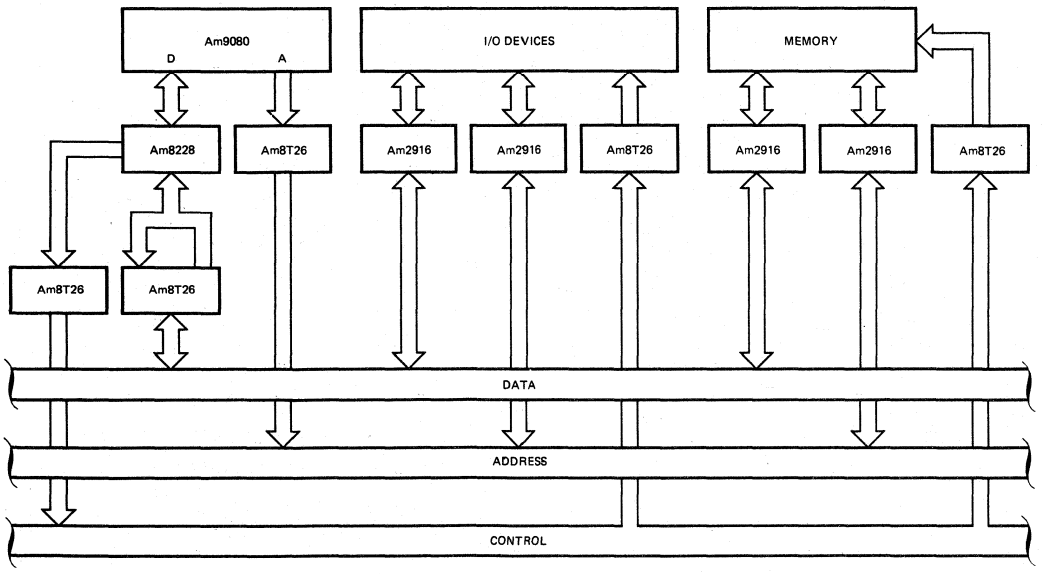
$\overline{RLE}$ Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

APPLICATIONS



Generating or checking parity for 16 data bits.



Using the Am2916 and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

Am2917

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- D-type register on driver
- Bus driver output can sink 40mA at 0.5V max
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2917 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

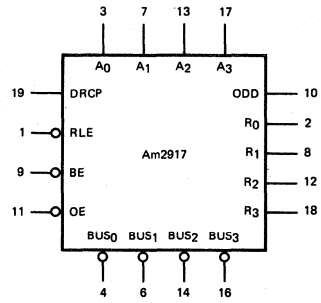
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

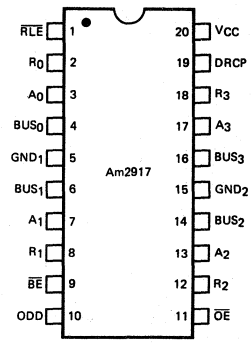
The Am2917 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

CONNECTION DIAGRAM
Top View



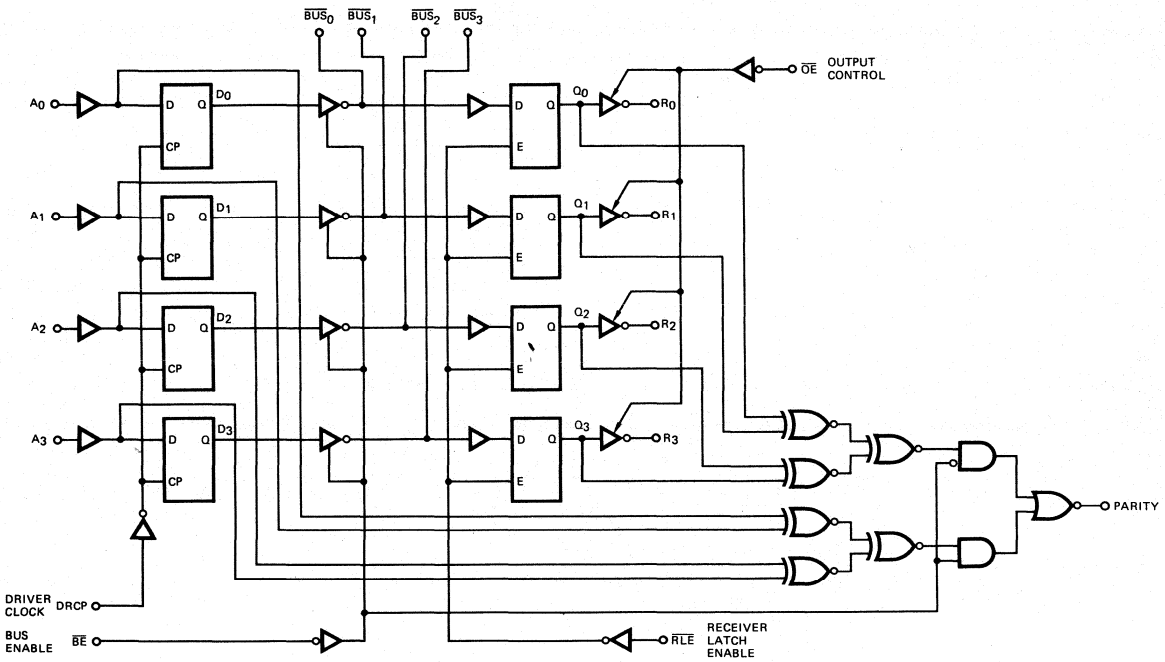
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2917PC
Hermetic DIP	0°C to +70°C	AM2917DC
Dice	0°C to +70°C	AM2917XC
Hermetic DIP	−55°C to +125°C	AM2917DM
*Hermetic Flat Pak	−55°C to +125°C	AM2917FM
Dice	−55°C to +125°C	AM2917XM

*Available on special order.

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	100 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917XC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75 V V_{CC}MAX. = 5.25 V

Am2917XM (MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50 V V_{CC}MAX. = 5.50 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24 mA			0.4	Volts
			I_{OL} = 40 mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	I_{OH} = −20 mA	2.4			Volts
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4 V	V_O = 0.4 V			−200	μA
			V_O = 2.4 V			50	
			V_O = 4.5 V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5 V V_{CC} = 0 V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4 V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4 V				0.8	Volts
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0 V		−50	−85	−130	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V

Am2917XM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		V_{CC} = 5.0 V, $I_{OH} = -100\mu$A		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu$A, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	

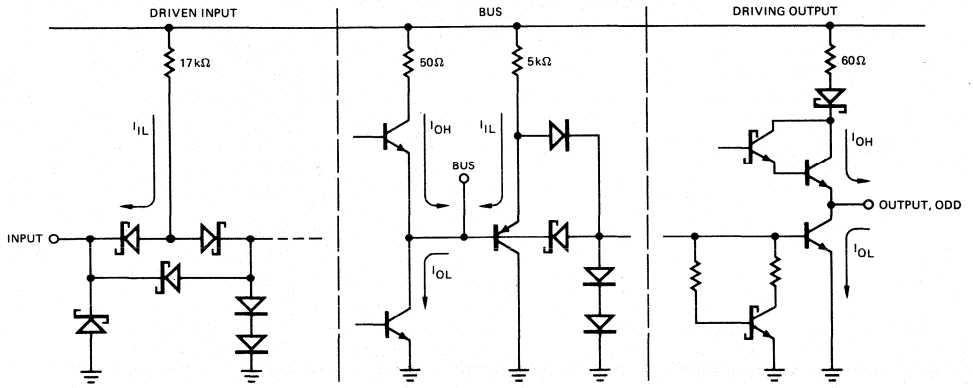
SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2917XM Min.	Am2917XM Typ. (Note 2)	Am2917XM Max.	Am2917XC Min.	Am2917XC Typ. (Note 2)	Am2917XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	26		13	23	
t_s	A Data Inputs		23			20			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	30		18	27	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	30		21	27	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)	C_L = 15pF, R_L = 2.0kΩ	11			14			ns
t_h			6.0			4.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{ZH}, t_{ZL}	Output Control to Output			14	26		14	23	ns
t_{HZ}, t_{LZ}				14	26		14	23	

PRELIMINARY
THESE SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

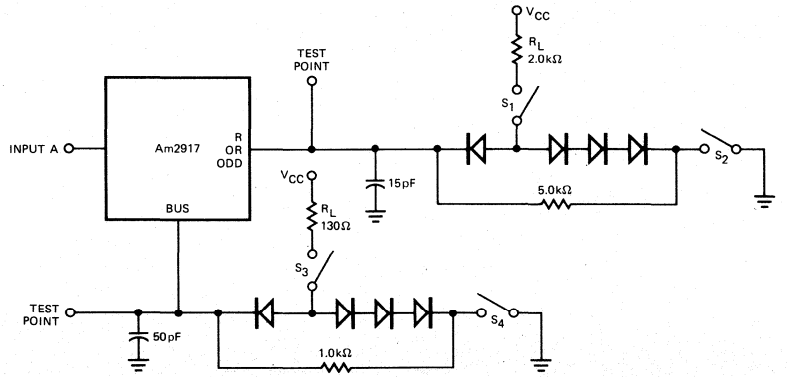
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

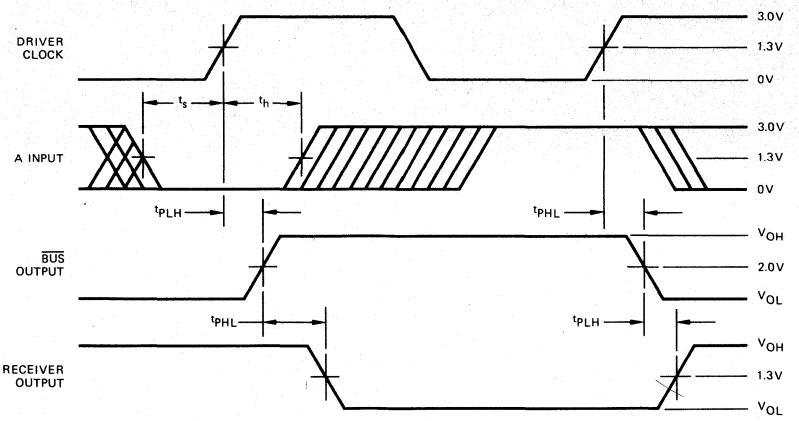


Note: Actual current flow direction shown.

SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

FUNCTION TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	BUS_i	R_i	
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

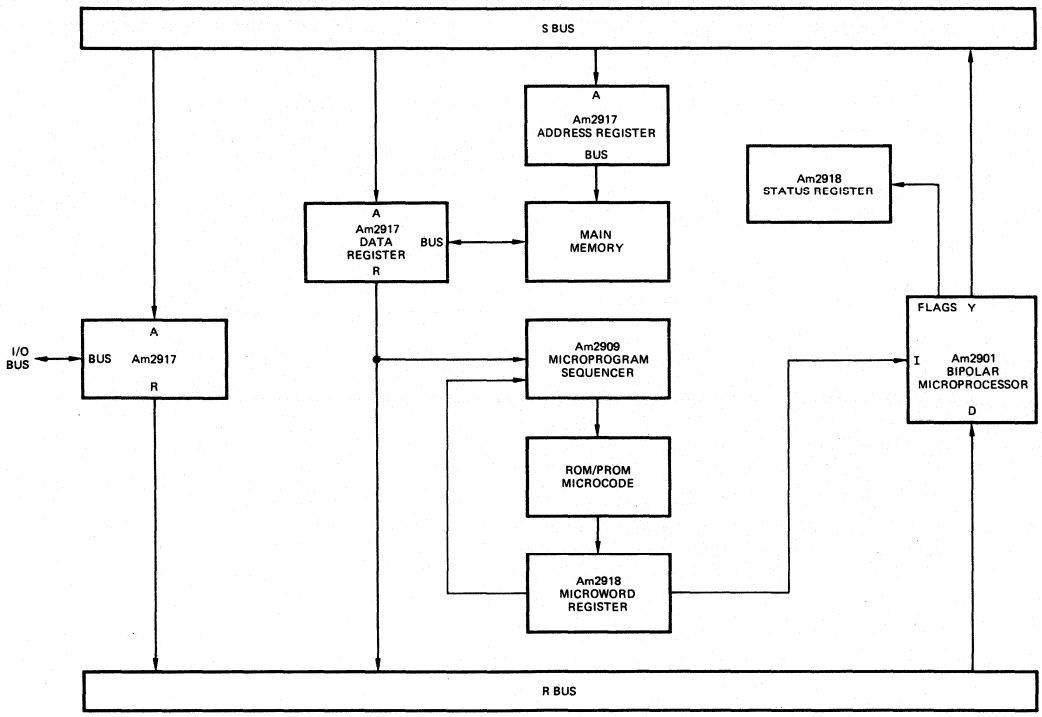
R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

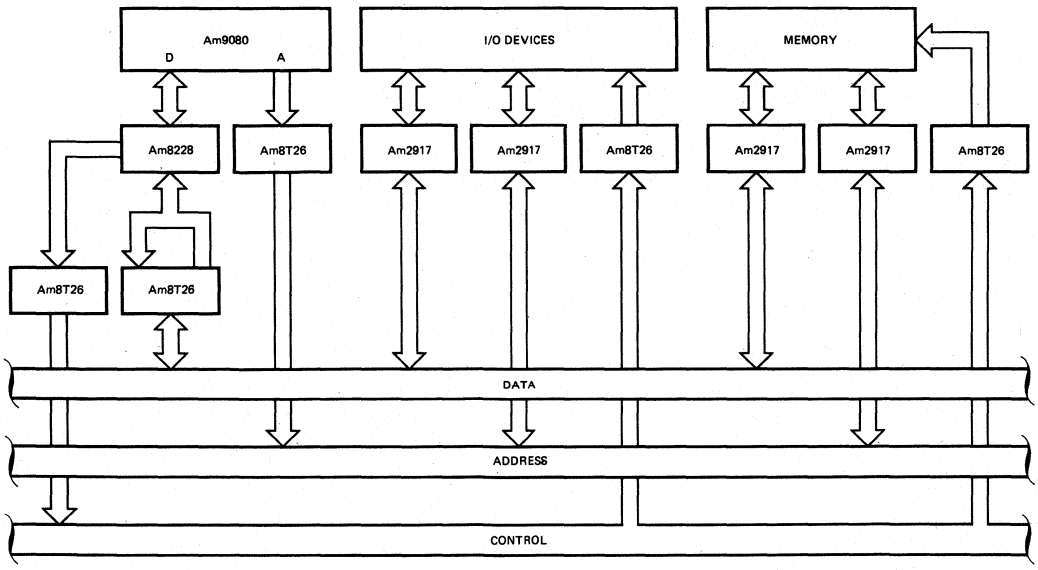
ODD Odd parity output.. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

APPLICATIONS



The Am2917 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.



Using the Am2917 and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

Am2918

Quad D Register With Standard And Three-State Outputs

Distinctive Characteristics

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency
- 100% reliability assurance testing in compliance with MIL-STD-883

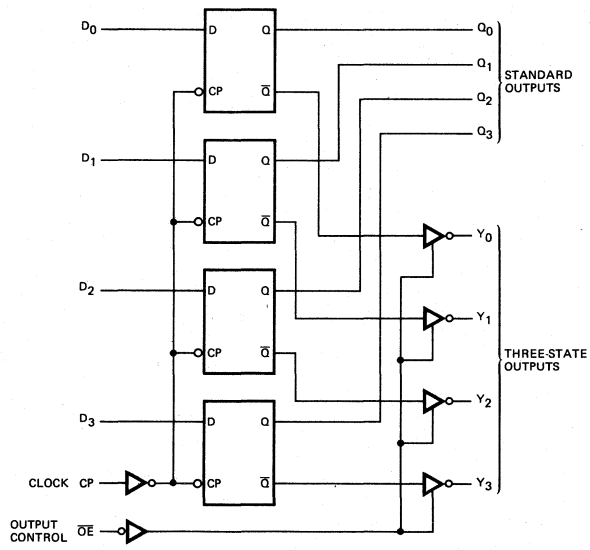
FUNCTIONAL DESCRIPTION

New Schottky circuits such as the Am2918 register provide the design engineer with additional flexibility in system configuration — especially with regard to bus structure, organization and speed. The Am2918 is a quadruple D-type register with four standard totem pole outputs and four three-state bus-type outputs. The 16-pin device also features a buffered common clock (CP) and a buffered common output control ($\overline{OE}$) for the Y outputs. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am2918 register can be used in bipolar microprocessor designs as an address register, status register, instruction register or for various data or microword register applications. Because of the unique design of the three-state output, the device features very short propagation delay from the clock to the Q or Y outputs. Thus, system performance and architectural design can be improved by using the Am2918 register. Other applications of Am2918 register can be found in microprogrammed display systems, communication systems and most general or special purpose digital signal processing equipment.

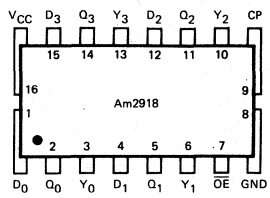
LOGIC DIAGRAM



ORDERING INFORMATION

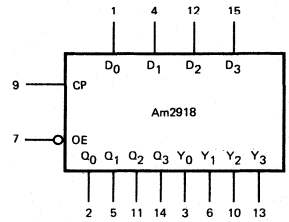
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2918PC
Hermetic DIP	0°C to +70°C	AM2918DC
Dice	0°C to +70°C	AM2918XC
Hermetic DIP	−55°C to +125°C	AM2918DM
Hermetic Flat Pack	−55°C to +125°C	AM2918FM
Dice	−55°C to +125°C	AM2918XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2918XC T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2918XM T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q	I_{OH} = −1mA MIL	2.5	3.4		Volts
				I_{OH} = −1mA COM'L	2.7	3.4		
			Y	XM, I_{OH} = −2mA	2.4	3.4		
				XC, I_{OH} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN., I_{OL} = 20mA; V_{IN} = V_{IH} or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−2.0	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					50	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX.		V_O = 2.4V			50	µA
				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				80	120	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test shoud not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V, R_L = 280Ω) For additional information, see pages 126 and 127.

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q Output	C_L = 15pF		6.0	9.0	ns
t_{PHL}				8.5	13	
t_{pw}	Clock Pulse Width		7.0			ns
t_s	Data		5.0			ns
t_h	Data		3.0			ns
t_{PLH}	Clock to Y Output ($\overline{OE}$ LOW)			6.0	9.0	ns
t_{PHL}				8.5	13	
t_{ZH}	Output Control to Output	C_L = 5pF		12.5	19	ns
t_{ZL}				12	18	
t_{HZ}		C_L = 50pF		4.0	6.0	
t_{LZ}				7.0	10.5	
f_{max}	Maximum Clock Frequency	C_L = 15pF	75	100		MHz

TRUTH TABLE

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

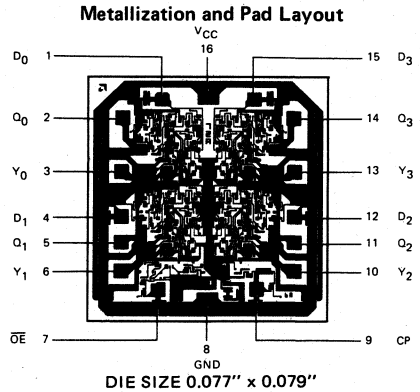
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_0	1	1	–	–
Q_0	2	–	20	10*
Y_0	3	–	40/130	10*
D_1	4	1	–	–
Q_1	5	–	20	10*
Y_1	6	–	40/130	10*
$\overline{OE}$	7	1	–	–
GND	8	–	–	–
CP	9	1	–	–
Y_2	10	–	40/130	10*
Q_2	11	–	20	10*
D_2	12	1	–	–
Y_3	13	–	40/130	10*
Q_3	14	–	20	10*
D_3	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

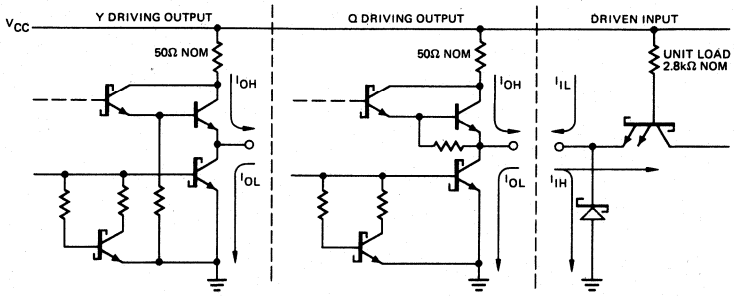
*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for i = 0, 1, 2, 3.

Metallization and Pad Layout



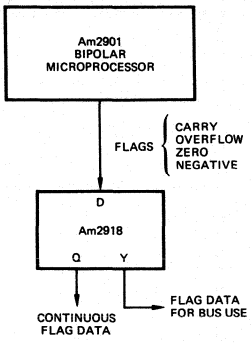
DIE SIZE 0.077" x 0.079"

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

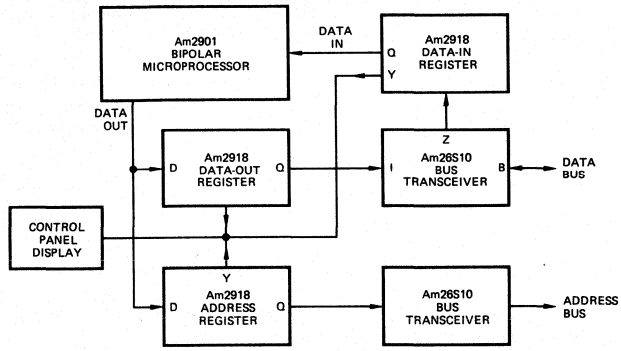


Note: Actual current flow direction shown.

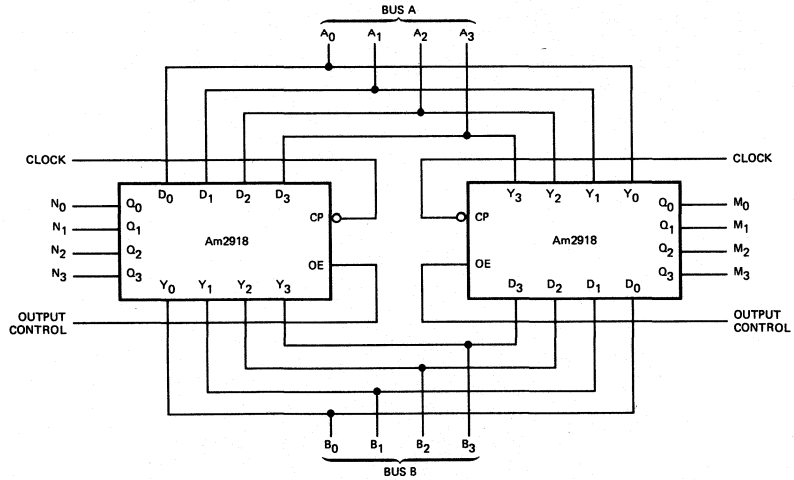
APPLICATIONS



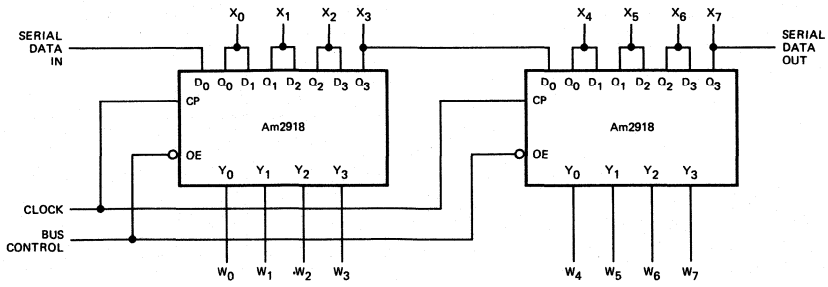
The Am2918 as a 4-Bit status register



The Am2918 used as data-in, data-out and address registers.



The Am2918 can be connected for bi-directional interface between two buses. The device on the left stores data from the A-bus and drives the A-bus. The device on the right stores data from the B-bus and drives the A-bus. The output control is used to place either or both drivers in the high-impedance state. The contents of each register are available for continuous usage at the N and M ports of the device.



8-Bit serial to parallel converter with three-state output (W) and direct access to the register word (X).

Am29700 • Am29701

Non-Inverting 64-Bit Random Access Memory

PRELIMINARY DATA

Distinctive Characteristics

- Fully decoded 16-word x 4-bit Schottky technology high-speed RAM.
- Access time typically 17ns.
- Non-inverting
- Available with three-state outputs (Am29701) or with open collector outputs (Am29700).
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

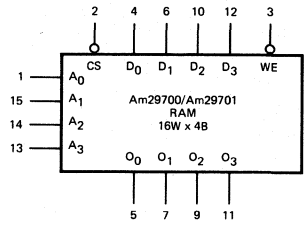
The Am29700 and Am29701 are 64-bit RAMs built using Schottky diode clamped transistors and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am29700) or three-state outputs (Am29701). Chip selection for large memory systems can be controlled by active LOW output decoders.

An active LOW Write line $\overline{WE}$ controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four outputs O_0 to O_3.

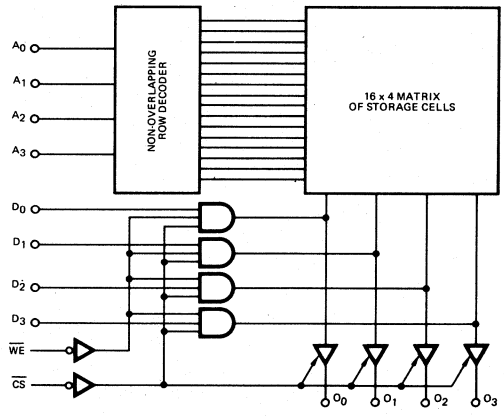
During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

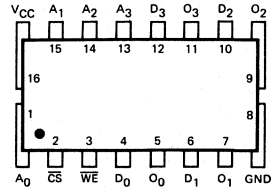
LOGIC BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collector Outputs		
Molded DIP	0°C to +75°C	AM29700PC
Hermetic DIP	0°C to +75°C	AM29700DC
Hermetic DIP	–55°C to +125°C	AM29700DM
Hermetic Flat Pak	–55°C to +125°C	AM29700FM
Three-State Outputs		
Molded DIP	0°C to +75°C	AM29701PC
Hermetic DIP	0°C to +75°C	AM29701DC
Hermetic DIP	–55°C to +125°C	AM29701DM
Hermetic Flat Pak	–55°C to +125°C	AM29701FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	100mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

Part Number	T_A	V_{CC}
Am29700PC, DC Am29701PC, DC	0°C to +75°C	5.0V ±5%
Am29700DM, FM Am29701DM, FM	−55°C to +125°C	5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am29701 Only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA		0.3	0.45	Volts
			I_{OL} = 20mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V	$\overline{WE}$, D_0–D_3, A_{0-3}		.030	0.25	mA
			$\overline{CS}$		.060	0.25	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				10	µA
I_{SC} (Am29701 Only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−20	−35	−60	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am29700		100		mA
			Am29701		100		
V_C	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −12mA				−1.5	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 2.4V	Am29700			100	µA
			Am29701			40	
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 0.4V, V_{CC} = MAX.	(Am29701)	−40			µA

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

1. Combinational Delays

Parameters	Description	Test Conditions	25°C Typ.	T_A = 0°C to +75°C Min.	Max.	Units
$t_{pd\pm}$ ($\overline{CS}$)	Delay Chip Select to Output HIGH or LOW	V_{CC} = 5.0V, C_L = 30pF, R_L = 300Ω V_{CC} and 600Ω to GND (16mA Load) measure at 1.5V PRELIMINARY DATA	10			ns
t_{pdz} ($\overline{CS}$)	Delay Chip Select HIGH to Output OFF		12			ns
t_{pd+} (A)	Delay Address to Output HIGH		17			ns
t_{pd-} (A)	Delay Address to Output LOW		17			ns
t_{rec} ($\overline{WE}$)	Write Recovery Time		18			ns
$t_{pd\pm}$ ($\overline{WE}$)	Delay $\overline{WE}$ HIGH to Output Active		18			ns
t_{pdz} ($\overline{WE}$)	Delay $\overline{WE}$ LOW to Output OFF		15			ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Cont.)

2. Set-up and Hold Requirements

Parameters	Description	Test Conditions	25°C Typ.	T_A = 0°C to +75°C Min.	Max.	Units
$t_{pw}(\overline{WE})$	Write Pulse Width	V_{CC} = 5.0V, C_L = 30pF, R_L = 300Ω V_{CC} and 600Ω to GND (16mA Load) measure at 1.5V PRELIMINARY DATA	18			ns
$t_s(D)$	Data Set-up Time		18			ns
$t_h(D)$	Data Hold Time		0			ns
$t_s(A)$	Address Set-up Time		0			ns
$t_h(A)$	Address Hold Time		0			ns

DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CS}$ Active LOW chip select input. When the chip select is LOW data can be read from or written into the memory.

D_i The data inputs of the memory, i = 1 – 4

O_i The data outputs of the memory, i = 1 – 4

$O_i(t_n)$ The state of output i at time n.

$D_i(t_{n-x})$ The state of the D_i input at time t_{n-x}, where t_{n-x} is the time of the last write operation into a given address.

$\overline{WE}$ Active LOW Write Enable. When the write enable is LOW, data on the data inputs is written into the addressed memory location. When $\overline{WE}$ is HIGH data is read from the addressed location and appears, inverted, at the O outputs.

UNIT LOAD A TTL input unit load is defined as –1.6mA at 0.4V (LOW state) and 40μA at 2.4V (HIGH state).

SWITCHING TERMS

$t_{pd\pm}(\overline{CS})$ The delay from the chip select input going LOW to the output going active.

$t_{pdz}(\overline{CS})$ The delay from the chip select going HIGH to the output assuming an inactive high impedance level.

$t_{pd\pm}(A)$ The delay from a change on the address inputs to a correct HIGH (t_{pd+}) or LOW (t_{pd-}) level on the outputs. Access time.

$t_{rec}(\overline{WE})$ Write recovery time. The delay from a LOW-to-HIGH transition on the write enable to the correct data on the outputs of the memory. This is the time required between the end of the write operation and a read operation in the same address.

$t_{pw}(\overline{WE})$ Minimum write pulse width. The LOW time on the write enable input required to cause a write.

$t_s(D)$, $t_h(D)$ Data set-up and hold times. The time, relative to the end of the write pulse (LOW-to-HIGH edge) after which the data on the data inputs will not be written into the memory. To ensure writing the correct data, the data must be present before $t_s(D)$ min. and must remain until after $t_h(D)$ min.

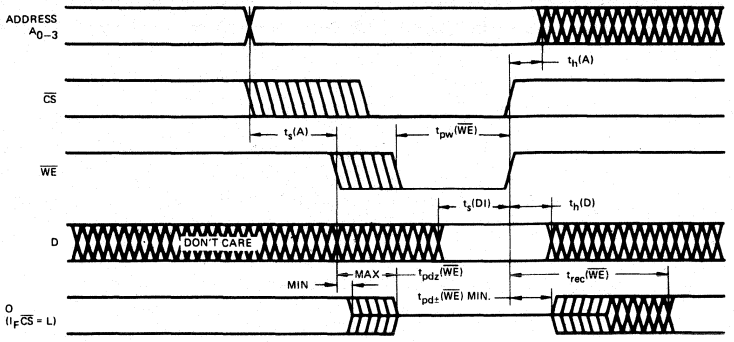
$t_s(A)$ Address set-up time. The time prior to the start of the write pulse (HIGH-to-LOW edge) at which the correct write address must be on the address inputs. An address change later than $t_s(A)$ max. may cause writing in two addresses.

$t_h(A)$ Address hold time. The time following the end of the write pulse (LOW-to-HIGH transition) at which a new address may be applied. An address change earlier than $t_h(A)$ min. may cause writing into two addresses.

$t_{pd\pm}(\overline{WE})$ The delay from a LOW-to-HIGH transition of the write enable to an active (but not necessarily correct) state on the data outputs. The correct state will be present after the write recovery time has elapsed.

$t_{pdo}(\overline{WE})$ The delay from a HIGH-to-LOW transition on the write enable to a high impedance level on the data outputs, if the chip is selected.

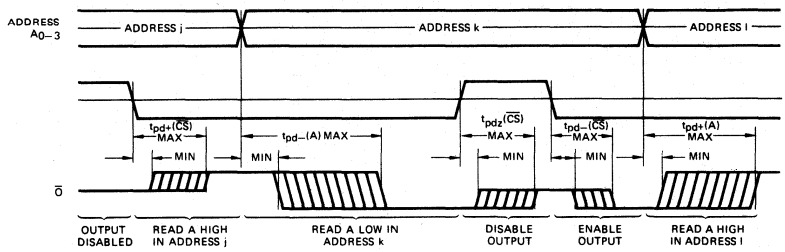
SWITCHING WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

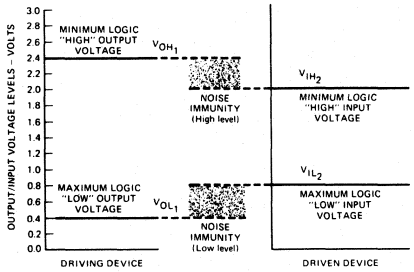
Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) min. must be allowed before the address may be changed again. The output will be inactive (floating for the Am29701) while the write enable is LOW. The three parameters t_s(A), t_h(A) and t_{pw}(WE) apply to the condition CS LOW AND WE LOW.

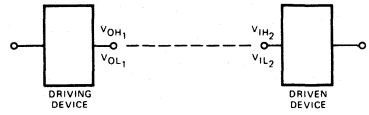


Switching delays from address and chip select inputs to the data output. For the Am29701 disabled output is "OFF", represented by a single center line. For the Am29700, a disabled output is HIGH.

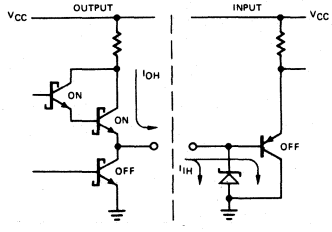
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



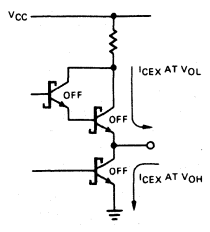


Current Conditions — HIGH State



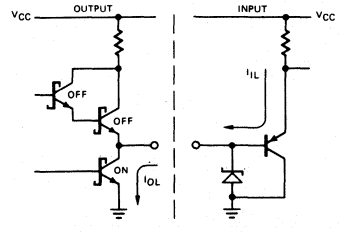
Note: Am29700 open collector.

Current Conditions — OFF State



Note: Am29700 open collector.

Current Conditions — LOW State



USER NOTES

1. The Am29701 output has active circuitry for both logic levels and requires no external pull-up resistor.
2. For a good DC noise margin with the Am29700 a pull-up resistor can be used. Limits of R in kΩ are given by

$$\frac{V_{CC} - V_{OH}\ \text{required}}{nI_{CEX} + NI_{IH}} > R_L > \frac{V_{CC} - V_{OL}\ \text{required}}{I_{OL} - NI_{IL}}$$

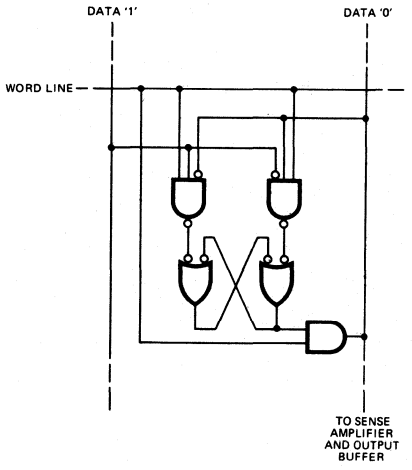
   Where n is number of OR tied outputs
   N is the number of TTL units loads driven.
3. Address and data lines can be interchanged within their respective groups for ease of P. C. layout without effecting device operation.
4. Since for a given pattern on the address lines reading and writing are performed on the same actual memory word, the address lines can be driven by any mixture of assertion or negation of the variables making up the address field.

LOADING RULES (In TTL Loads)

Input/Output	Pin No.'s	Input Loading	Output Drive (Am29701) HIGH	LOW
A_0	1	0.16	–	–
$\overline{CS}$	2	0.16	–	–
$\overline{WE}$	3	0.16	–	–
D_0	4	0.16	–	–
O_0	5	–	20	10
D_1	6	0.16	–	–
O_1	7	–	20	10
GND	8	–	–	–
O_2	9	–	20	10
D_2	10	0.16	–	–
O_3	11	–	20	10
D_3	12	0.16	–	–
A_3	13	0.16	–	–
A_2	14	0.16	–	–
A_1	15	0.16	–	–
V_{CC}	16	–	–	–

A TTL unit load is −1.6mA at 0.4V and 40μA at 2.0V.
The Am29700 has open collector outputs; the output drive in the HIGH state is determined by an external pull-up resistor.

BASIC MEMORY CELL



TRUTH TABLE

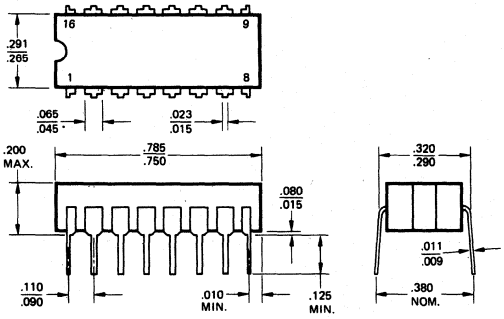
INPUTS $\overline{CS}$	INPUTS $\overline{WE}$	INPUTS D_i	OUTPUTS $O_i(t_n)$	MODE
H	L	L	Off	No Selection
H	L	H	Off	No Selection
H	H	X	Off	No Selection
L	L	L	Off	Write '0'
L	L	H	Off	Write '1'
L	H	X	$D_i(t_{n-x})$	Read

H = HIGH Voltage Level
L = LOW Voltage Level
OFF = HIGH Impedance

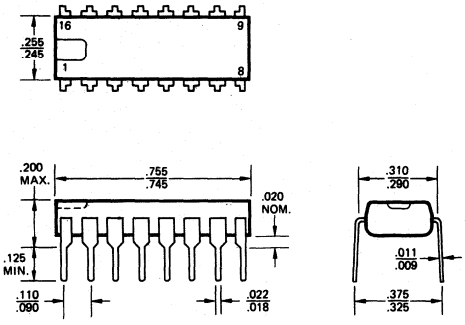
Note: The Am29700 output is at a high impedance level at all times except when reading a LOW.

PHYSICAL DIMENSIONS
Dual-In-Line

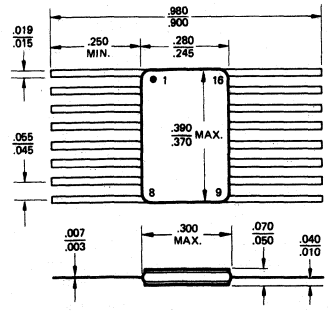
Hermetic



Molded



Flat Package



Am29702 • Am29703

Inverting 64-Bit Random Access Memories

PRELIMINARY DATA

Distinctive Characteristics

- Fully decoded 16-word x 4-bit Schottky technology high-speed RAM.
- Access time typically 17ns.
- Non-Inverting outputs
- Available with three-state outputs (Am29703) or with open collector outputs (Am29702).
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

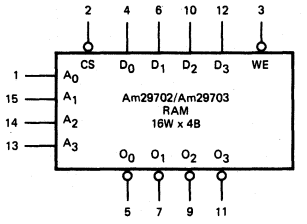
The Am29702 and Am29703 are 64-bit RAMs built using Schottky diode clamped transistors and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am29702) or three-state outputs (Am29703). Chip selection for large memory systems can be controlled by active LOW output decoders.

An active LOW Write line $\overline{WE}$ controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_0$ to $\overline{O}_3$.

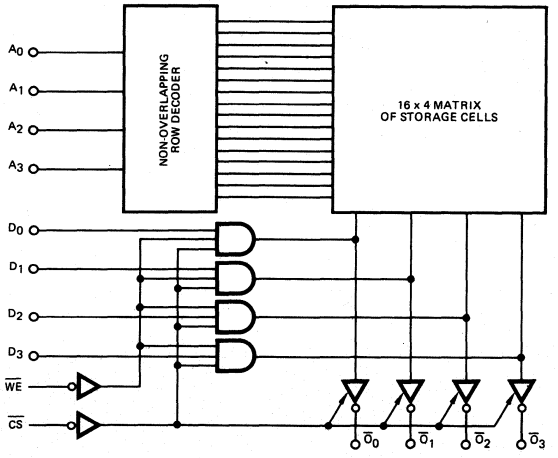
During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

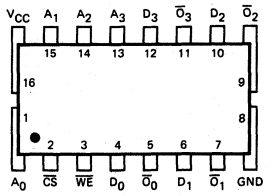
LOGIC BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collector Outputs		
Molded DIP	0°C to +75°C	AM29702PC
Hermetic DIP	0°C to +75°C	AM29702DC
Hermetic DIP	–55°C to +125°C	AM29702DM
Hermetic Flat Pak	–55°C to +125°C	AM29702FM
Three-State Outputs		
Molded DIP	0°C to +75°C	AM29703PC
Hermetic DIP	0°C to +75°C	AM29703DC
Hermetic DIP	–55°C to +125°C	AM29703DM
Hermetic Flat Pak	–55°C to +125°C	AM29703FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	100mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

Part Number	T_A	V_{CC}
Am29702PC, DC Am29703PC, DC	0°C to +75°C	5.0V ±5%
Am29702DM, FM Am29703DM, FM	−55°C to +125°C	5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am29703 Only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA		0.3	0.45	Volts
			I_{OL} = 20mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX.,	$\overline{WE}$, D_0–D_3, A_{0-3}		.030	0.25	mA
		V_{IN} = 0.45V	$\overline{CS}$		.060	0.25	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				10	μA
I_{SC} (Am29703 Only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−20	−35	−60	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am29702		100		mA
			Am29703		100		
V_C	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −12mA				−1.5	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}	Am29702			100	μA
		V_{OUT} = 2.4V	Am29703			40	
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 0.4V, V_{CC} = MAX.	(Am29703)	−40			μA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

1. Combinational Delays

Parameters	Description	Test Conditions	25°C Typ.	T_A = 0°C to +75°C Min.	Max.	Units
$t_{pd\pm}$ ($\overline{CS}$)	Delay Chip Select to Output HIGH or LOW	V_{CC} = 5.0V, C_L = 30pF, R_L = 300Ω V_{CC} and 600Ω to GND (16mA Load) measure at 1.5V	10			ns
t_{pdz} ($\overline{CS}$)	Delay Chip Select HIGH to Output OFF		12			ns
t_{pd+} (A)	Delay Address to Output HIGH		17			ns
t_{pd-} (A)	Delay Address to Output LOW		17			ns
t_{rec} ($\overline{WE}$)	Write Recovery Time		18			ns
$t_{pd\pm}$ ($\overline{WE}$)	Delay $\overline{WE}$ HIGH to Output Active	PRELIMINARY DATA	18			ns
t_{pdz} ($\overline{WE}$)	Delay $\overline{WE}$ LOW to Output OFF		15			ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Cont.)

2. Set-up and Hold Requirements

Parameters	Description	Test Conditions	25°C Typ.	T_A = 0°C to +75°C Min.	Max.	Units
$t_{pw}(\overline{WE})$	Write Pulse Width	V_{CC} = 5.0V, C_L = 30pF, R_L = 300Ω V_{CC} and 600Ω to GND (16mA Load) measure at 1.5V PRELIMINARY DATA	18			ns
$t_s(D)$	Data Set-up Time		18			ns
$t_h(D)$	Data Hold Time		0			ns
$t_s(A)$	Address Set-up Time		0			ns
$t_h(A)$	Address Hold Time		0			ns

DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CS}$ Active LOW chip select input. When the chip select is LOW data can be read from or written into the memory.

D_i The data inputs of the memory, i = 1 – 4

O_i The data outputs of the memory, i = 1 – 4

$O_i(t_n)$ The state of output i at time n.

$D_i(t_{n-x})$ The state of the D_i input at time t_{n-x}, where t_{n-x} is the time of the last write operation into a given address.

$\overline{WE}$ Active LOW Write Enable. When the write enable is LOW, data on the data inputs is written into the addressed memory location. When $\overline{WE}$ is HIGH data is read from the addressed location and appears, inverted, at the $\overline{O}$ outputs.

UNIT LOAD A TTL input unit load is defined as –1.6mA at 0.4V (LOW state) and 40μA at 2.4V (HIGH state).

SWITCHING TERMS

$t_{pd\pm}(\overline{CS})$ The delay from the chip select input going LOW to the output going active.

$t_{pdz}(\overline{CS})$ The delay from the chip select going HIGH to the output assuming an inactive high impedance level.

$t_{pd\pm}(A)$ The delay from a change on the address inputs to a correct HIGH (t_{pd+}) or LOW (t_{pd-}) level on the outputs. Access time.

$t_{rec}(\overline{WE})$ Write recovery time. The delay from a LOW-to-HIGH transition on the write enable to the correct data on the outputs of the memory. This is the time required between the end of the write operation and a read operation in the same address.

$t_{pw}(\overline{WE})$ Minimum write pulse width. The LOW time on the write enable input required to cause a write.

$t_s(D)$, $t_h(D)$ Data set-up and hold times. The time, relative to the end of the write pulse (LOW-to-HIGH edge) after which the data on the data inputs will not be written into the memory. To ensure writing the correct data, the data must be present before $t_s(D)$ min. and must remain until after $t_h(D)$ min.

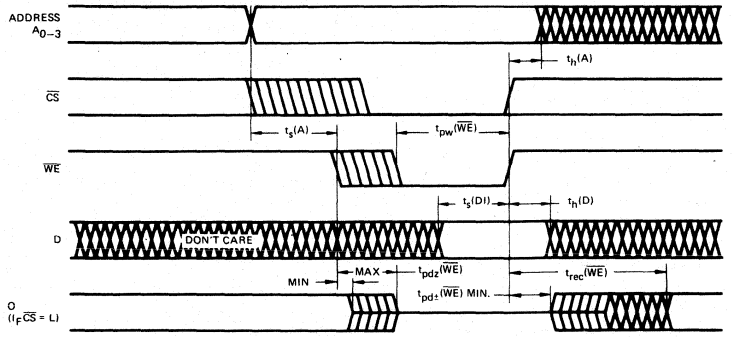
$t_s(A)$ Address set-up time. The time prior to the start of the write pulse (HIGH-to-LOW edge) at which the correct write address must be on the address inputs. An address change later than $t_s(A)$ max. may cause writing in two addresses.

$t_h(A)$ Address hold time. The time following the end of the write pulse (LOW-to-HIGH transition) at which a new address may be applied. An address change earlier than $t_h(A)$ min. may cause writing into two addresses.

$t_{pd\pm}(\overline{WE})$ The delay from a LOW-to-HIGH transition of the write enable to an active (but not necessarily correct) state on the data outputs. The correct state will be present after the write recovery time has elapsed.

$t_{pdo}(\overline{WE})$ The delay from a HIGH-to-LOW transition on the write enable to a high impedance level on the data outputs, if the chip is selected.

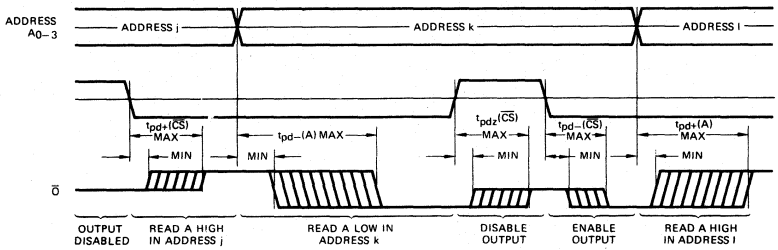
SWITCHING WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

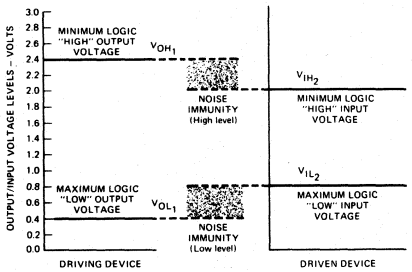
Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min. must be allowed before the address may be changed again. The output will be inactive (floating for the Am29703) while the write enable is LOW. The three parameters $t_s(A)$, $t_h(A)$ and $t_{pw}(WE)$ apply to the condition CS LOW AND WE LOW.

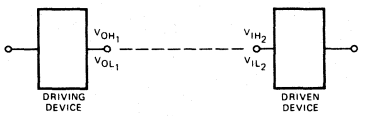


Switching delays from address and chip select inputs to the data output. For the Am29703 disabled output is "OFF", represented by a single center line. For the Am29702, a disabled output is HIGH.

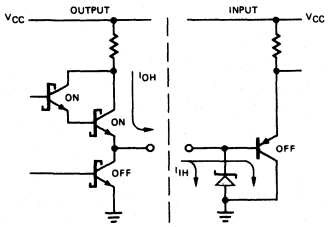
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



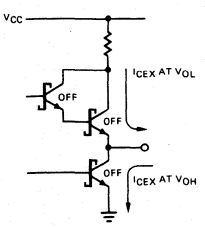


Current Conditions — HIGH State



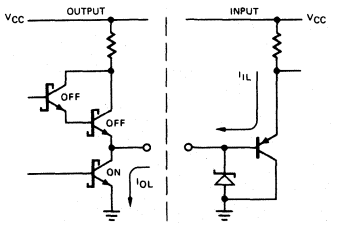
Note: Am29702 is open collector.

Current Conditions — OFF State



Note: Am29702 is open collector.

Current Conditions — LOW State



USER NOTES

1. The Am29703 output has active circuitry for both logic levels and requires no external pull-up resistor.
2. For a good DC noise margin with the Am29702 a pull-up resistor can be used. Limits of R in kΩ are given by

$$\frac{V_{CC} - V_{OH}\text{ required}}{nI_{CEX} + NI_{IH}} > R_L > \frac{V_{CC} - V_{OL}\text{ required}}{I_{OL} - NI_{IL}}$$

   Where n is number of OR tied outputs
   N is the number of TTL units loads driven.

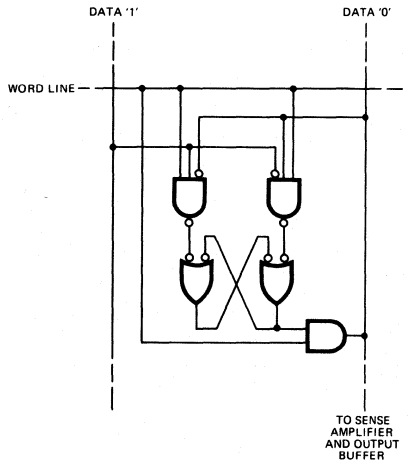
3. Address and data lines can be interchanged within their respective groups for ease of P. C. layout without effecting device operation.
4. Since for a given pattern on the address lines reading and writing are performed on the same actual memory word, the address lines can be driven by any mixture of assertion or negation of the variables making up the address field.

LOADING RULES (In TTL Loads)

Input/Output	Pin No.'s	Input Loading	Output Drive (Am29703) HIGH	LOW
A_0	1	0.16	–	–
$\overline{CS}$	2	0.16	–	–
$\overline{WE}$	3	0.16	–	–
D_0	4	0.16	–	–
$\overline{O}_0$	5	–	20	10
D_1	6	0.16	–	–
$\overline{O}_1$	7	–	20	10
GND	8	–	–	–
$\overline{O}_2$	9	–	20	10
D_2	10	0.16	–	–
$\overline{O}_3$	11	–	20	10
D_3	12	0.16	–	–
A_3	13	0.16	–	–
A_2	14	0.16	–	–
A_1	15	0.16	–	–
V_{CC}	16	–	–	–

A TTL unit load is −1.6mA at 0.4V and 40μA at 2.0V.
The Am29702 has open collector outputs; the output drive in the HIGH state is determined by an external pull-up resistor.

BASIC MEMORY CELL



TRUTH TABLE

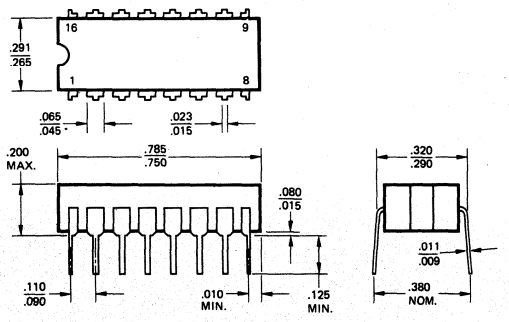
INPUTS $\overline{CS}$	INPUTS $\overline{WE}$	INPUTS D_i	OUTPUTS $\overline{O}_i(t_n)$	MODE
H	L	L	Off	No Selection
H	L	H	Off	No Selection
H	H	X	Off	No Selection
L	L	L	Off	Write '0'
L	L	H	Off	Write '1'
L	H	X	$\overline{D}_i(t_{n-x})$	Read

H = HIGH Voltage Level
L = LOW Voltage Level
OFF = HIGH Impedance

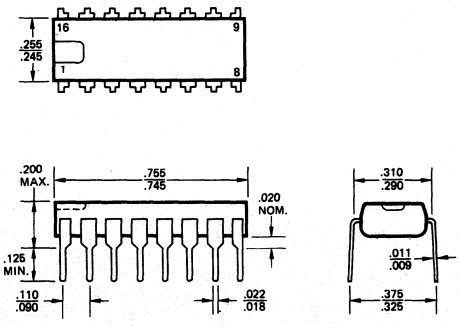
Note: The Am29702 output is at a high impedance level at all times except when reading a LOW.

PHYSICAL DIMENSIONS
Dual-In-Line

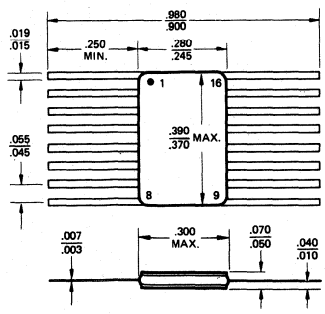
Ceramic



Molded



Flat Package



Am29704 • Am29705

16-Word By 4-Bit Two-Port RAM

Distinctive Characteristics

- 16-word by 4-bit, 2-port RAM
- Two output ports, each with separate output control
- Separate four-bit latches on each output port
- Data output is non-inverting with respect to data input
- Chip Select and Write Enable inputs for ease in cascading
- Advanced Low-Power Schottky processing
- 100% reliability testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

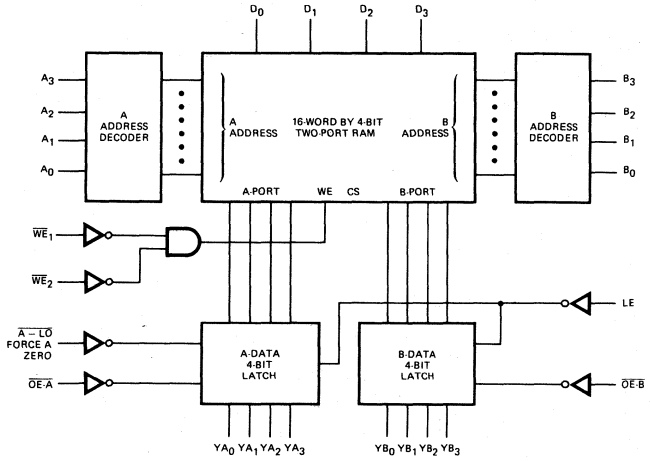
The Am29704 and Am29705 are 16-word by 4-bit, two-port RAM's built using advanced Low-Power Schottky processing. These RAM's feature two separate output ports such that any two 4-bit words can be read from these outputs simultaneously. Each output port has a four-bit latch but a common Latch Enable (LE) input is used to control all eight latches. The device has two Write Enable ($\overline{WE}$) inputs and is designed such that the Write Enable 1 ($\overline{WE}_1$) and Latch Enable (LE) inputs can be wired together to make the operation of the RAM appear edge triggered.

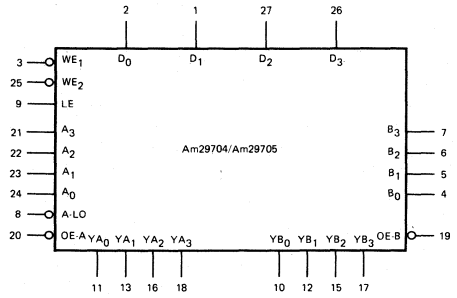
The device has a fully decoded four-bit A-address field to address any of the 16 memory words for the A-output port. Likewise, a four-bit B-address input is used to simultaneously select any of the 16 words for presentation at the B-output port. New incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load new data into the device.

The Am29704 has open-collector outputs and the Am29705 features three-state outputs so that several devices can be cascaded to increase the total number of memory words in the system. The A-output port is in the high-impedance state when the $\overline{OE}$-A input is HIGH. Likewise, the B-output port is in the high-impedance state when the $\overline{OE}$-B input is HIGH. Four devices can be paralleled using only one Am25LS139 decoder for output control.

The Write Enable inputs control the writing of new data into the RAM. When both Write Enable inputs are LOW, new data is written into the word selected by the B-address field. When either Write Enable input is HIGH, no data is written into the RAM. The memory outputs follow the data inputs during writing.

LOGIC DIAGRAM AND LOGIC SYMBOL



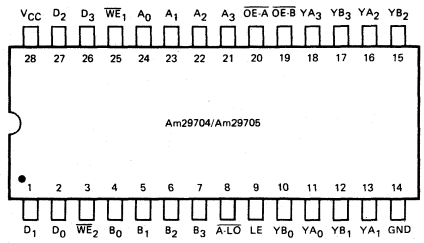


V_{CC} = Pin 28
GND = Pin 14

ORDERING INFORMATION

Package Type	Temperature Range	Open-Collector Order Number	Three-State Order Number
Molded DIP	0°C to +70°C	AM29704PC	AM29705PC
Hermetic DIP	0°C to +70°C	AM29704DC	AM29705DC
Dice	0°C to +70°C	AM29704XC	AM29705XC
Hermetic DIP	−55°C to +125°C	AM29704DM	AM29705DM
Hermetic Flat Pak	−55°C to +125°C	AM29704FM	AM29705FM
Dice	−55°C to +125°C	AM29704XM	AM29705XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am29704XC, Am29705XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am29704XM, Am29705XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Am29705 Only)	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4			Volts
			COM'L, I_{OH} = −4.0mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	A_i, B_i			−0.2	mA
			Others			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				0.1	mA
I_O	Output OFF Current (Am29705 Only)	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = V_{IH} or V_{IL}				100	µA
I_O	Off State (High Impedance) Output Current (Am29705 Only)	V_{CC} = MAX., V_{IN} = V_{IH} or V_{IL}	V_o = 2.7V			20	µA
			V_o = 0.4V			−20	
I_{SC}	Output Short Circuit Current (Note 3) (Am29705 Only)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			110	177	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS (Input Levels = 0V and 3.0V, Transitions Measured at 1.3V)

Combinational Delays (in ns) (R_L = 2.0kΩ, C_L = 15pF)

Parameters	From	To	Conditions	T_A = 25°C, V_{CC} = 5.0V Typ.	Max.	T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Max.	T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Max.
Access Time	A Address Stable	YA Stable	LE = HIGH	23			
	B Address Stable	YB Stable		23			
	Both $\overline{WE}$ LOW	YA = D	LE = HIGH, A = B	32			
		YB = D	LE = HIGH	32			
Turn-On Time	$\overline{OE\text{-}A}$ or $\overline{OE\text{-}B}$ LOW	YA or YB Stable		15			
Turn-Off Time	$\overline{OE\text{-}A}$ or $\overline{OE\text{-}B}$ HIGH	YA or YB Off		15			
Reset Time	$\overline{A\text{-}LO}$ LOW	YA LOW		22			
Enable Time	LE HIGH	YA and YB Stable		18			
	Data In	YA or YB = D	LE = HIGH, $\overline{WE}$ both LOW, A = B				

PRELIMINARY
THESE SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

SWITCHING CHARACTERISTICS (Cont.)

(Input Levels = 0V and 3.0V, Transitions Measured at 1.3V)

Minimum Set-up and Hold Times (in ns)

Parameters	From	To	Conditions	$T_A = 25°C$ $V_{CC} = 5.0V$ Typ.	Max.	$T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ Max.	$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ Max.
Data Set-up Time	D Stable	Either $\overline{WE}$ HIGH		30			
Data Hold Time	Either $\overline{WE}$ HIGH	D Changing		0			
Address Set-up Time	B Stable	Both $\overline{WE}$ LOW		0			
Address Hold Time	Either $\overline{WE}$ HIGH	B Changing		0			
Latch Close Before Write Begins	LE LOW	$\overline{WE}_1$ LOW	$\overline{WE}_2$ LOW	0			
	LE LOW	$\overline{WE}_2$ LOW	$\overline{WE}_1$ LOW	0			
Address Set-up Before Latch Closes	A or B Stable	LE LOW		23			

PRELIMINARY
THESE SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

Minimum Pulse Widths

Parameters	Input	Pulse	Conditions	$T_A = 25°C$ $V_{CC} = 5.0V$ Typ.	Max.	$T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ Max.	$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ Max.
Write Pulse Width	$\overline{WE}_1$	HIGH-LOW-HIGH	$\overline{WE}_2$ LOW	25			
	$\overline{WE}_2$	HIGH-LOW-HIGH	$\overline{WE}_1$ LOW	25			
A Latch Reset Pulse	$\overline{A\text{-}LO}$	HIGH-LOW-HIGH		20			
Latch Data Capture	LE	LOW-HIGH-LOW	Address Stable	15			

FUNCTION TABLES

WRITE CONTROL

$\overline{WE}_1$	$\overline{WE}_2$	Function	RAM Outputs at Latch Inputs A-Port	B-Port
L	L	Write D Into B	A data (A ≠ B)	D input data
X	H	No write	A data	B data
H	X	No write	A data	B data

H = HIGH
L = LOW
X = Don't care

YA READ

Inputs $\overline{OE-A}$	Inputs $\overline{A-LO}$	Inputs LE	YA Output	Function
H	X	X	Z	High impedance
L	L	X	L	Force YA LOW
L	H	H	A – Port RAM data	Latches transparent
L	H	L	NC	Latches retain data

H = HIGH
L = LOW
X = Don't care
Z = High impedance
NC = No change

YB READ

Inputs $\overline{OE-B}$	Inputs LE	YB Output	Function
H	X	Z	High impedance
L	H	B – Port RAM data	Latches transparent
L	L	NC	Latches retain data

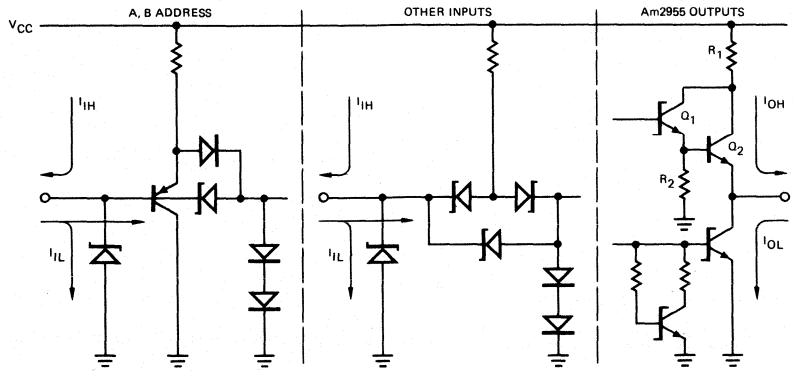
H = HIGH
L = LOW
X = Don't care
Z = High impedance
NC = No change

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_1	1	1	–	–
D_0	2	1	–	–
$\overline{WE}_1$	3	1	–	–
B_0	4	0.55	–	–
B_1	5	0.55	–	–
B_2	6	0.55	–	–
B_3	7	0.55	–	–
$\overline{A-LO}$	8	1	–	–
LE	9	1	–	–
YB_0	10	–	100/200	33
YA_0	11	–	100/200	33
YB_1	12	–	100/200	33
YA_1	13	–	100/200	33
GND	14	–	–	–
YB_2	15	–	100/200	33
YA_2	16	–	100/200	33
YB_3	17	–	100/200	33
YA_3	18	–	100/200	33
$\overline{OE-B}$	19	1	–	–
$\overline{OE-A}$	20	1	–	–
A_3	21	0.55	–	–
A_2	22	0.55	–	–
A_1	23	0.55	–	–
A_0	24	0.55	–	–
$\overline{WE}_2$	25	1	–	–
D_3	26	1	–	–
D_2	27	1	–	–
V_{CC}	28	–	–	–

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.
Omit Q_1, Q_2, R_1 and R_2 for Am29704.

DEFINITION OF TERMS

D_0, D_1, D_2, D_3 Data Inputs. New data is written into the RAM through these inputs.

A_0, A_1, A_2, A_3 The A-address Inputs. The four-bit field presented at the A inputs selects one of the 16 memory words for presentation to the A-Data Latch.

B_0, B_1, B_2, B_3 The B-address inputs. The four-bit field presented at the B inputs selects one of the 16 memory words for presentation to the B-Data Latch. The B address field also selects the word into which new data is written.

YA_0, YA_1, YA_2, YA_3 The four A-Data Latch Outputs.

YB_0, YB_1, YB_2, YB_3 The four B-Data Latch Outputs.

$\overline{WE}_1, \overline{WE}_2$ Write Enables. When both Write Enables are LOW, new data is written into the word selected by the B-address field. If either Write Enable input is HIGH, no new data can be written into the memory.

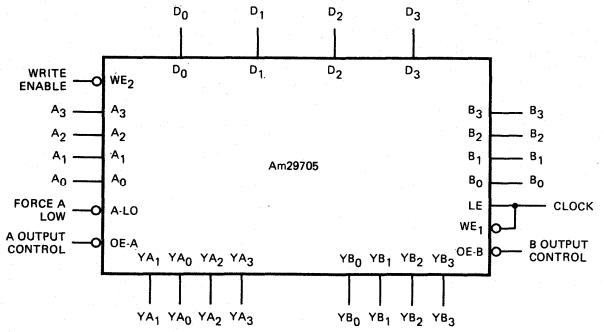
$\overline{OE\text{-}A}$ A-port Output Enable. When $\overline{OE\text{-}A}$ is LOW, data in the A-Data Latch is present at the YA_i outputs. If $\overline{OE\text{-}A}$ is HIGH, the YA_i outputs are in the high-impedance (off) state.

$\overline{OE\text{-}B}$ B-port Output Enable. When $\overline{OE\text{-}B}$ is LOW, data in the B-Data Latch is present at the YB_i outputs. When $\overline{OE\text{-}B}$ is HIGH, the YB_i outputs are in the high-impedance (off) state.

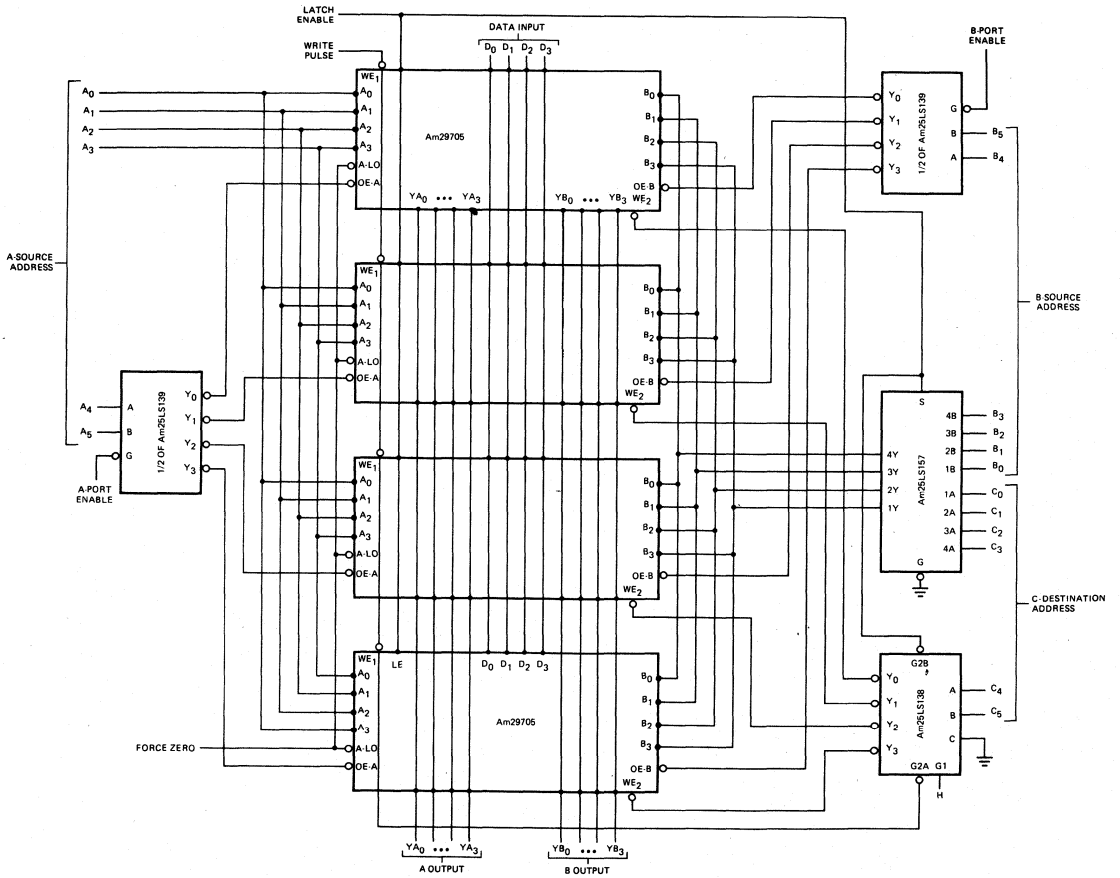
LE Latch Enable. The LE input controls the latches for both the RAM A-output port and RAM B-output port. When the LE input is HIGH, the latches are open (transparent) and data from the RAM, as selected by the A and B address fields, is present at the outputs. When LE is LOW, the latches are closed and they retain the last data read from the RAM independent of the current A and B address field inputs.

$\overline{A\text{-}LO}$ Force A Zero. This input is used to force the outputs of the A-port latches LOW independent of the Latch Enable input or A-address field select inputs. Thus, the A-output bus can be forced LOW using this control signal. When the $\overline{A\text{-}LO}$ input is HIGH, the A latches operate in their normal fashion. Once the A latches are forced LOW, they remain LOW independent of the $\overline{A\text{-}LO}$ input if the latches are closed.

APPLICATIONS

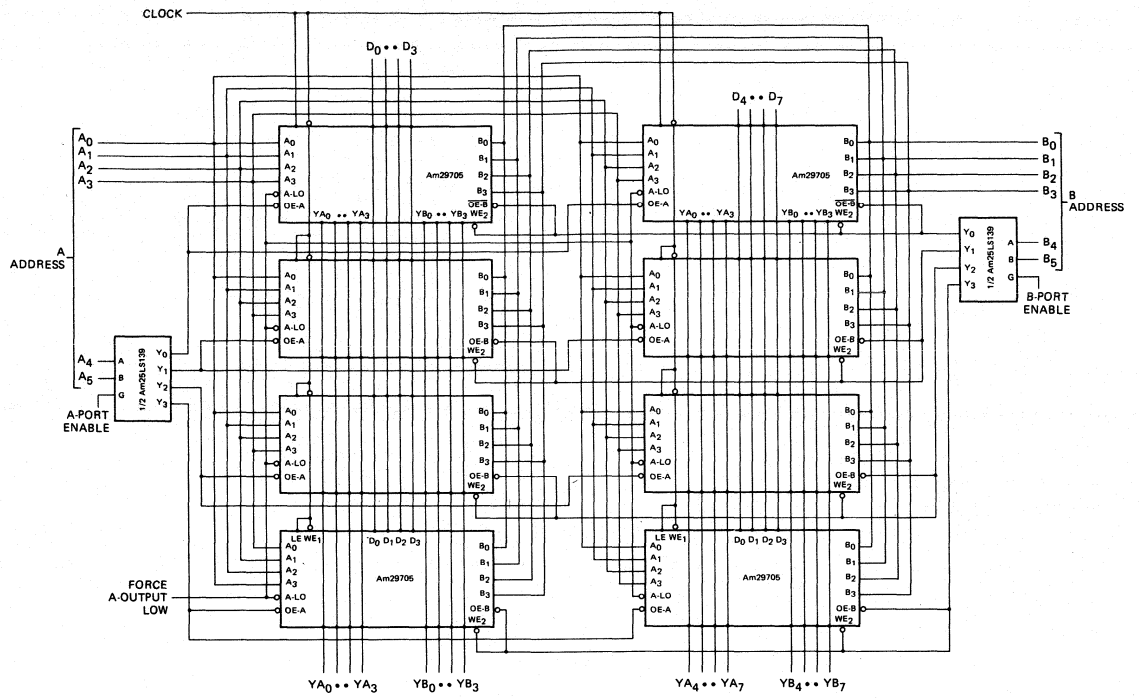


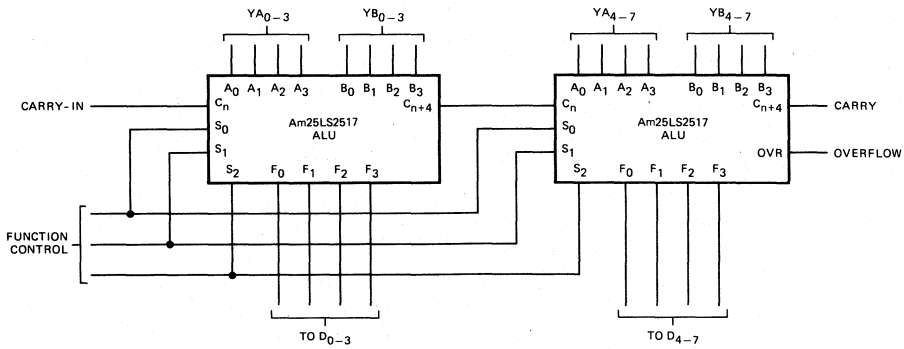
A 16-word by 4-bit two-port RAM with LE and $\overline{WE}_1$ connected to make the device appear edge triggered.



A 64-word by 4-bit three address memory. Data is read from the A address to the YA outputs and from the B address to the YB outputs while the latch enable is HIGH. When the latch enable goes LOW, the YA and YB data is held in the internal latches, and the RAM B address is switched to the C-destination address lines. A write pulse will then deposit the input data into the location selected by the C address.

APPLICATIONS (Cont'd)

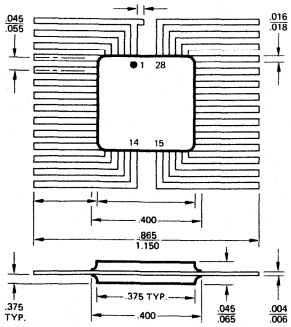




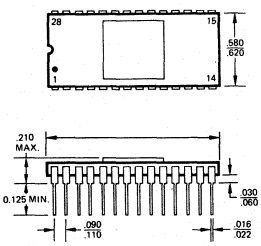
64-word by 8-bit two-port memory and ALU.

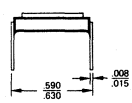
PHYSICAL DIMENSIONS
Dual-In-Line

28-Pin Flat Package

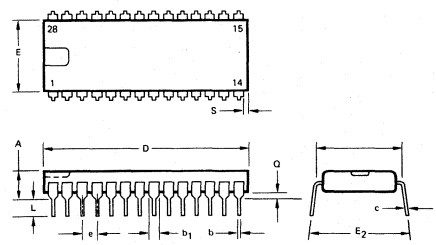


28-Pin Side Brazed





28-Pin Ceramic



Am29720 • Am29721

Low-Power Schottky 256-Bit Random Access Memories

DISTINCTIVE CHARACTERISTICS

- Fully decoded 256-bit TTL RAMs.
  Plug-in replacements for 74200, IM5503/5523, 93411/21
  Pin compatible with MM6530/31, 3106/7, 82S06, 74S201
- Open collector (Am29720) and three-state (Am29721)
- High speed operation:
  35ns typical access time
  45ns guaranteed (0°C to +75°C)
  55ns guaranteed (–55°C to +125°C)
- Very low power dissipation
  275mW typical
  70mA maximum I_{CC}
- Full military temperature range performance.
  10% power supply tolerance
- Internal ECL circuitry
  Uniform access times over voltage and temperature variations.
- Tested to GALPAT.
  Functional and switching characteristics are guaranteed for all data and address patterns.

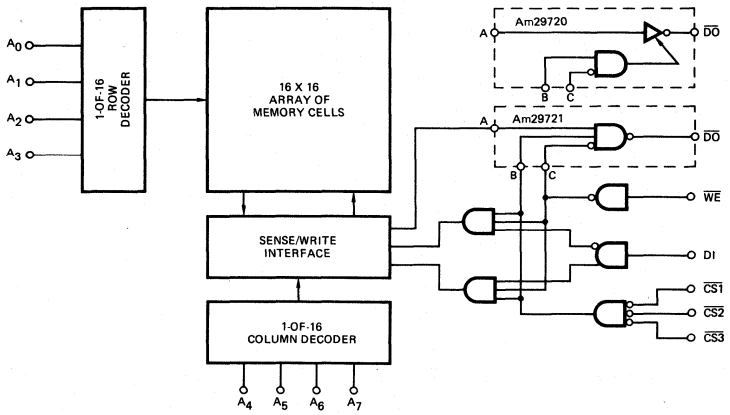
FUNCTIONAL DESCRIPTION

The Am29720 and Am29721 are fully decoded bipolar random access memories for use in high-speed buffer memories and as a replacement for high-speed core memories in digital systems. The memories are organized 256-words by 1-bit with an 8-bit binary address field and separate data in and data output lines. The memories have three active LOW chip select inputs and a three-state output (Am29721) or open-collector output (Am29720). All inputs are buffered to present an input load of only 0.5 TTL unit loads.

Read/write operation is controlled by an active LOW write enable input. When the write enable is LOW and the chip is selected the data on the data input is written into the location specified by the address inputs. During this operation the output floats allowing the data bus to be used by other memories or open-collector logic elements that are tied to the inverting data output. Reading is accomplished by having the chip selected and the write enable input HIGH. Data stored in the location specified by the address inputs is read out and appears on the data output inverted.

The chip is selected by three active LOW inputs all of which must be LOW in order for the data output to be active during the read operation and for data to be written into or from the memory. These three active LOW chip select inputs permit the Am25LS138 MSI decoders to select memories in either a linear select, two or three dimensional mode of operation when large memory systems are being built. The delay from the chip select to the output is considerably faster than from the address inputs and extra delay can be tolerated in the chip select path without affecting system performance.

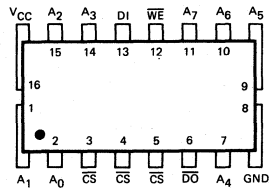
LOGIC DIAGRAM



ORDERING INFORMATION

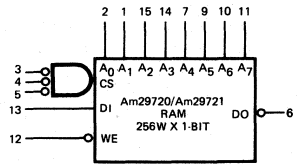
Three-State Output		
Molded DIP	0°C to +75°C	AM29721PC
Hermetic DIP	0°C to +75°C	AM29721DC
Hermetic DIP	–55°C to +125°C	AM29721DM
Flat Pack	–55°C to +125°C	AM29721FM
Open Collector Output		
Molded DIP	0°C to +75°C	AM29720PC
Hermetic DIP	0°C to +75°C	AM29720DC
Hermetic DIP	–55°C to +125°C	AM29720DM
Flat Pack	–55°C to +125°C	AM29720FM

CONNECTION DIAGRAM
Top View



Note:
Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +V_{CC}
Output Current, Into Outputs	30mA
DC Input Current	−30mA to +50mA

OPERATING RANGE

Part No.	Ambient Operating Temperature	Power Supply Voltage
Am29720DC, PC Am29721DC, PC	0°C to +75°C	4.75 V to 5.25 V
Am29720DM, FM Am29721DM, FM	−55°C to +125°C	4.50 V to 5.50 V

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage (Am29721 Only)	V_{CC} = MIN., I_{OH} = −2.0 mA (MIL Range) V_{IN} = V_{IH} or V_{IL}, I_{OH} = −2.6 mA (COM'L Range)	2.4	3.1		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA, V_{IN} = V_{IH} or V_{IL}		0.3	0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−0.50	−0.80	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V		<1	20	μA
V_{BK}	Input Breakdown Voltage	V_{CC} = MAX., I_{IN} = 100 μA	7.0			V
I_{LK}	Output Leakage Current	V_{CC} = MAX., $\overline{CS}$ = 2.4 V, V_{OUT} = 2.4 V		<1	30	μA
		V_{CC} = MAX., $\overline{CS}$ = 2.4 V, V_{OUT} = 0.4 V		<1	−30	
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−20	−30	−60	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		55	70	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18 mA			−1.5	Volts

Note 1. Typical Limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description		T_A = 25°C Typ.	T_A = 0°C to 75°C Min.	T_A = 0°C to 75°C Max.	T_A = −55°C to 125°C Min.	T_A = −55°C to 125°C Max.	Units
t_{PLH}(A) t_{PHL}(A)	Delay from Address to Output	See Fig. 2	35	15	45	10	55	ns
t_{PZH}($\overline{CS}$) t_{PZL}($\overline{CS}$)	Delay from Chip Select to Active Output and Correct Data	See Fig. 2	15	5	25	5	30	ns
t_{PHZ}($\overline{CS}$) t_{PLZ}($\overline{CS}$)	Delay from Chip Select to Inactive Output	See Fig. 2	15	5	25	5	30	ns
t_{rec}($\overline{WE}$)	Delay from Write Enable (HIGH) to Correct Output Data	See Fig. 1	25		45		55	ns
t_{PZH}($\overline{WE}$) t_{PZL}($\overline{WE}$)	Delay from Write Enable (HIGH) to Active Output	See Fig. 1		5		5		ns
t_{PHZ}($\overline{WE}$) t_{PLZ}($\overline{WE}$)	Delay from Write Enable (LOW) to Inactive Output	See Fig. 1	20		30		40	ns
t_s(A)	Set-up Time Address	See Fig. 1	0	0		5		ns
t_h(A)	Hold Time Address		0	0		5		ns
t_s(DI)	Set-up Time Data Input	See Fig. 1	20	30		35		ns
t_h(DI)	Hold Time Data Input	See Fig. 1	0	0		5		ns
t_{pw}($\overline{WE}$)	Write Enable Pulse Width	See Fig. 1	20	30		35		ns

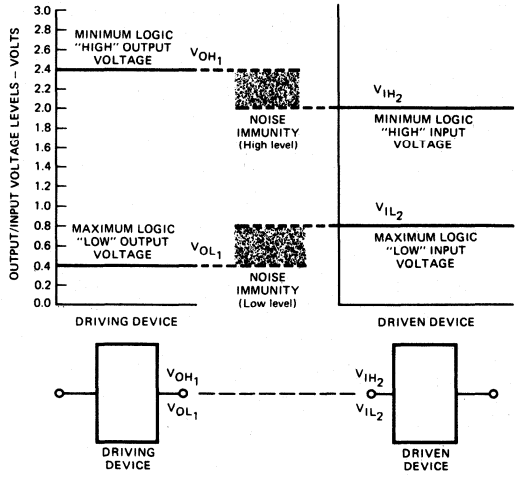
Am29720/Am29721 LOADING RULES (In TTL Unit Loads)

Input/Output	Pin No.s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
A_1	1	0.5	—	—
A_0	2	0.5	—	—
$\overline{CS}$	3	0.5	—	—
$\overline{CS}$	4	0.5	—	—
$\overline{CS}$	5	0.5	—	—
DO	6	—	(Note) 50	10
A_4	7	0.5	—	—
GND	8	—	—	—
A_5	9	0.5	—	—
A_6	10	0.5	—	—
A_7	11	0.5	—	—
$\overline{WE}$	12	0.5	—	—
DI	13	0.5	—	—
A_3	14	0.5	—	—
A_2	15	0.5	—	—
V_{CC}	16	—	—	—

Note: Am2950 has open collector output.

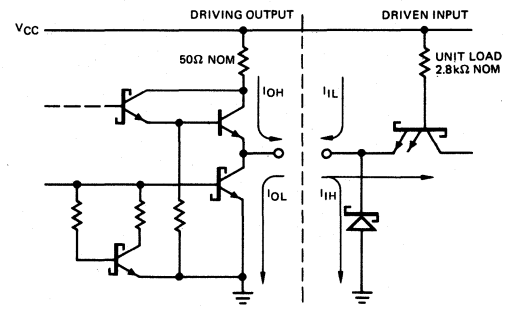
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions – LOW & HIGH



Note: Refer to Electrical Characteristics for measure currents.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

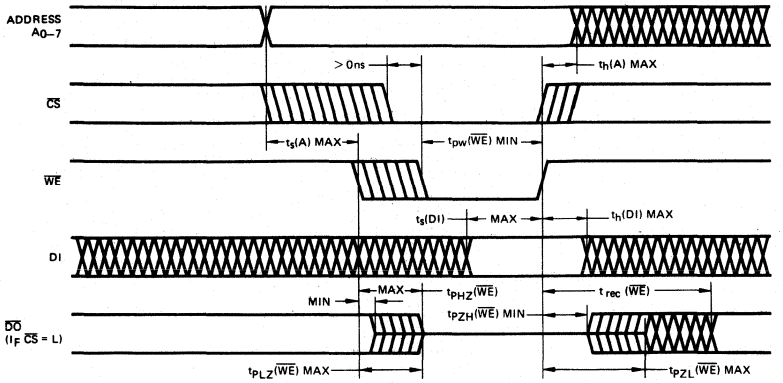
Note: 1. 54L/74L has two different types of standard inputs.

TRUTH TABLE

Inputs $\overline{CS}$	Inputs $\overline{WE}$	Inputs DI	Output $\overline{DO}(t_{n+l})$	Mode
H	X	X	OFF	No Selection
L	L	L	OFF	Write '0'
L	L	H	OFF	Write '1'
L	H	X	$\overline{DI}(t_n)$	Read

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
OFF = Floating output level is determined by external circuitry connected to the output.

SWITCHING WAVEFORMS

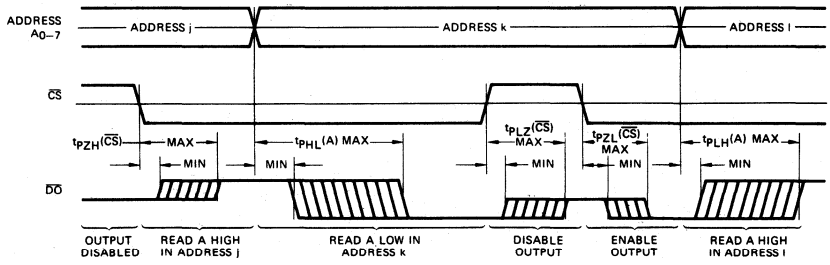


KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) max., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) max. must be allowed before the address may be changed again. The output will be inactive (floating for the Am29721) while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.

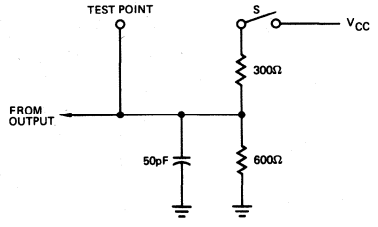
Figure 1



Switching delays from address and chip select inputs to the data output. For the Am29721 disabled output is "OFF," represented by a single center line. For the Am29720, a disabled output is HIGH.

Figure 2

TEST LOAD



Note: All measurements at 1.5 V.

S is closed for all tests except for Am29721 tests in which the output switches between an active HIGH level and a HIGH impedance state.

OUTPUT LOADING RULES

The Am29720 has an open collector output. The outputs of several memories may be tied together and the common line connected through a pull-up resistor to V_{CC}. The common line will go LOW if and only if one of the Am29720 outputs connected to it goes LOW, i.e., is enabled and reading a LOW. The HIGH state is established by the pull-up resistor. The value of the resistor is limited by two equations:

$$R(min) = \frac{V_{CC}\,(max) - 0.4}{16 - i\,(1.6)}$$

i = number of TTL inputs driven

$$R(max) = \frac{V_{CC}\,(min) - 2.4}{0.03n + 0.04i}$$

n = number of Am2950 outputs connected together

For highest speed, use the minimum R; for lowest power, use the maximum R.

The Am29721 has active circuitry to establish both the HIGH and LOW logic levels and requires no pull-up resistor. Up to 64 Am29721 outputs can be connected together.

DEFINITIONS OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH-signal level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to a LOW signal level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

X Unknown or don't care state

Z OFF, applying to the third high impedance state of the output.

FUNCTIONAL TERMS:

Three State A three state output can exist in three possible states: output LOW sinking current, output HIGH sourcing current, and output floating where the output level is determined by external circuitry connected to the output. This three state output allows AND tying of memory outputs for memory expansion and still keeps the inherent high speed of active pull-up circuitry.

Fully Decoded In a fully decoded memory every possible address combination of logic HIGH's and LOW's uniquely selects a memory word. This form of decoding requires no additional special purpose decoders for system operation and is the most efficient in terms of address inputs required and overall system speed.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level).

t_{PXH} The delay from a logic level change at an input to a HIGH level on an output.

t_{PXL} The delay from a logic level change at an input to a LOW level on an output.

t_{PXZ} The delay from a logic level change at an input to a high impedance state on a three state output. Measured with a resistor pull-down or pull-up.

t_{PXX}**(A)** The delay from an address input to the memory output.

t_{PXX}**(**$\overline{\text{CS}}$**)** The delay from a chip select input to the memory output.

t_{PXZ}**(**$\overline{\text{WE}}$**)** The delay from a HIGH-to-LOW transition on the write enable to a high impedance level on the memory output.

t_{PZX}**(**$\overline{\text{WE}}$**)** The delay from a LOW-to-HIGH transition on the write enable to an active level on the memory output.

t_{pw}**(**$\overline{\text{WE}}$**)** The shortest LOW pulse on the write enable input which is guaranteed to cause the memory to write. Pulses shorter than $t_{pw}(\overline{WE})$ min. may or may not cause a write to occur.

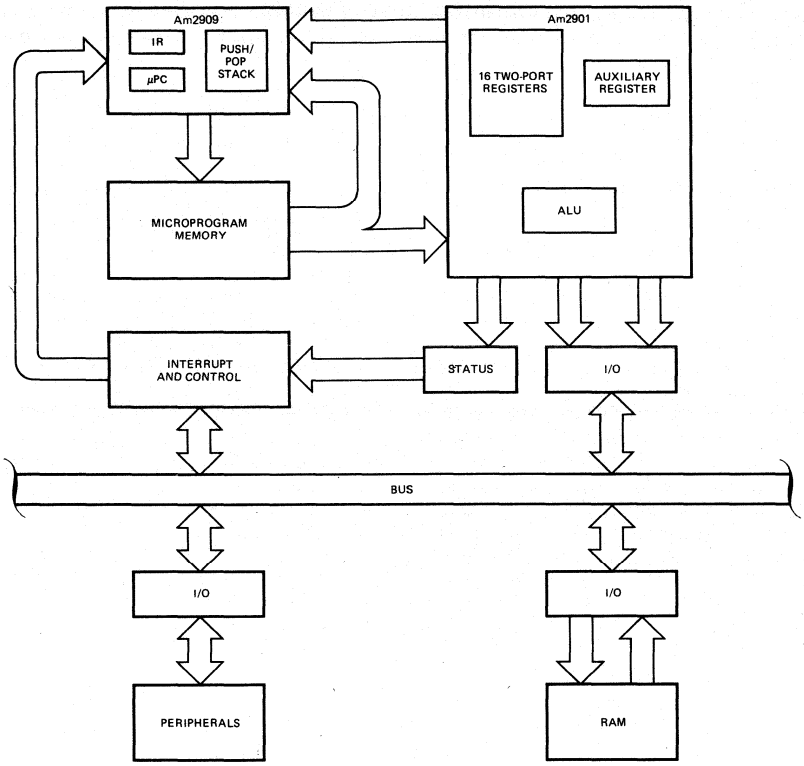
t_s**(A)** The set-up time of the address inputs relative to the HIGH-to-LOW edge of the write pulse. This is the time required for internal address decoding to settle. To avoid writing in spurious addresses, a stable address should be applied to the address inputs at least $t_s(A)$ max. before the write pulse begins.

t_h**(A)** The address hold time. This parameter is similar to $t_s(A)$ but is measured relative to the end of the write pulse rather than the beginning. A stable address should be maintained on the address inputs for $t_h(A)$ max. after the write pulse has ended in order to prevent writing in spurious addresses.

t_s**(DI)** Data set-up time. The time prior to the end of the write pulse during which data must be stable to be correctly written into the memory.

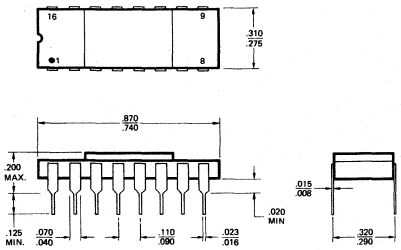
t_h**(DI)** Data hold time. The time following the end of the write pulse during which data must not be changed.

BIPOLAR MICROCOMPUTER ARCHITECTURE

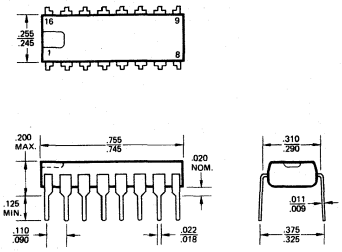


PHYSICAL DIMENSIONS

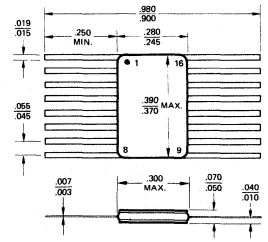
16-Pin Side Brazed DIP



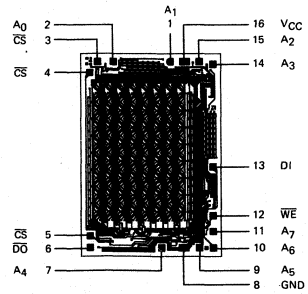
16-Pin Molded DIP



16-Pin Flat Pack



Metallization and Pad Layout



DIE SIZE 84 X 121 Mils

Am29750 • Am29751

32-Word By 8-Bit PROM's

Distinctive Characteristics

- Field programmable read only memory
- Highly reliable polysilicon fuses
- Pin compatible with types IM5600/5610, 82S23/123, MM5330/31, SN74188 and HPROM 8256
- Typical fusing time of 200 μs/bit
- 50 ns access time
- Three-state and open-collector versions

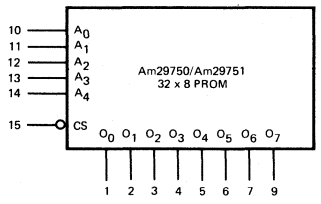
FUNCTIONAL DESCRIPTION

The Am29750 and Am29751 are electrically programmable Schottky TTL read only memories. Both devices are organized as 32 words of 8 bits each; the Am29750 has open collector outputs and the Am29751 has three-state outputs. The devices are shipped with all bits HIGH and each bit in the memory can be programmed to a LOW by applying appropriate voltages to the circuit. At each bit location on the circuit there is a narrow link of polysilicon material which is conductive, but which can be opened like a fuse by passing a short, high-current pulse through it. The fusing process simply melts the polysilicon at the center of the link and the two melted ends pull away from each other insuring a very reliable open circuit, which produces a LOW at the memory output.

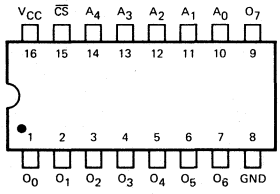
The programming voltage is applied at the output pin for the bit to be programmed, while the word to be programmed is selected by normal TTL levels on the address lines. The passage of current through the link is controlled by a programming pulse on the chip select input. There are two extra words and one additional bit for each word on the chip which are programmed at the factory during testing to insure high programming yields in devices shipped.

After programming, the device can be used for microprogram storage or random logic function generation, like any read-only memory. If the chip select input is held HIGH, the outputs will all turn off, so the outputs of several memories can be tied together for expansion.

LOGIC SYMBOL



CONNECTION DIAGRAM
Top View

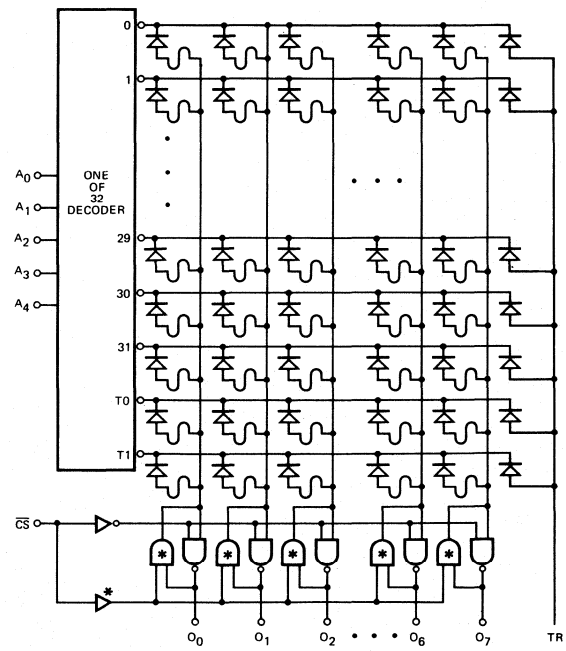


Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM29750DC
Hermetic DIP	−55°C to +125°C	AM29750DM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM29751DC
Hermetic DIP	−55°C to +125°C	AM29751DM

BLOCK DIAGRAM



* = High Voltage Gate for Programming
T0 = Test Word
T1 = Test Word
TR = Test Rail

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Input Voltage (Address Inputs)	−0.5V to +5.5V
DC Voltage Applied to Outputs During Programming	25V
Output Current into Outputs During Programming	125 mA
DC Input Voltage (Chip Select Input)	−0.5V to +15.5V

OPERATING RANGE

Am29750DC, Am29751DC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
Am29750DM, Am29751DM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am29751 Only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.3	0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V			−0.030	−0.25	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				20	μA
I_{SC} (Am29751 Only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−12	−35	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.	Am29750		78	100	mA
			Am29751		87	110	
V_C	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −5.0mA				−1.0	V
I_{CEX}	Output Leakage Current	Am29750	V_O = V_{CC}, $V_{\overline{CS}}$ = 2.4V			100	μA
		Am29751	V_O = 2.4V or 0.4V	−40		40	
			$V_{\overline{CS}}$ = 2.4V				

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

				V_{CC}=5.0V T_A=25°C		V_{CC} = 5.0V±5% T_A=0° to +70°C		V_{CC} = 5.0V ±10% T_A=−55°C to +125°C		
Parameter	Description	Test Conditions		Typ.	Max.	Typ.	Max.	Typ.	Max.	Units
t_{EN}	Delay Chip Select to Output Active HIGH or LOW	C_L = 30 pF R_L = 300Ω to VCC and 600Ω to GND (16mA Load) Note 2	Am29750	22	30	30	40	45	60	ns
			Am29751	28	35	30	40	45	60	
t_{DIS}	Delay Chip Select HIGH to Output OFF		Am29750	22	30	30	40	45	60	ns
			Am29751	28	35	30	40	45	60	
t_{pd+}(A)	Delay Address to Output HIGH			32	50	40	55	55	75	ns
t_{pd-}(A)	Delay Address to Output LOW			32	50	40	55	55	75	ns

Note 2. 300Ω resistor opened for t_{DIS} and t_{EN} measurements between HIGH and LOW states.

PROGRAMMING THE Am29750 and Am29751

The Am29750 and Am29751 are shipped with a polysilicon fusible link at each bit location. The output of the memory with the link in place is HIGH. To program the device the fusible links are selectively opened; reading an open location produces a LOW at the memory output.

The link is opened by passing a large current through it from a voltage supply of 20 V on the memory output. The current is directed through the fuse by raising the chip select input to 15 volts. After a short programming pulse, the 20-volt supply is removed, the chip is enabled, and the output level is sensed to determine whether or not the link has opened. If it has not opened another programming sequence is initiated on the output and chip select lines. If the link has opened – that is, a LOW is sensed – the programming pulses are continued for 100 μsec to insure that the bit has been programmed reliably.

Most links will open with a few one microsecond programming pulses. Occasionally a link will be a little stronger and will require longer programming pulse. The duration of the programming pulse may be gradually lengthened up to 8 μsec until a total elapsed time of 100msec has been spent on one bit. A link which has not opened by 100ms is most likely defective, and further programming of the device should not be attempted.

The memories will become hot during the programming due to the large currents being passed. Programming pulses should not be applied to one device more than 1.6 seconds to avoid heat damage. If this programming time is ever exceeded, all power to the chip, including V_{CC}, should be removed for a period of 300ms, after which programming can continue in cycles of 200 ms programming and 300 ms power off.

TEST WORDS

The Am29750 and Am29751 have an extra ninth bit on each word and two extra words. These extra locations are used by Advanced Micro Devices for testing purposes. The ninth bit on each word is accessible only on the die, and cannot be examined on packaged units. The two test words can be accessed on packaged units by applying a special address condition. The two test words are intended for AMD use only and will already be programmed in parts shipped. However, users may wish to access these test words for their own testing.

There is also a special address condition which forces all memory outputs to the LOW state, allowing verification of output LOW characteristics prior to programming.

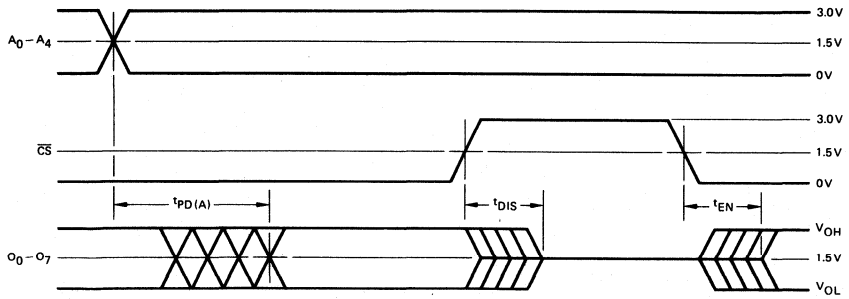
INPUTS (VOLTS)						OUTPUTS
$\overline{CS}$	A_4	A_3	A_2	A_1	A_0	$O_7 - O_0$
0.4	X	13±1	13±1	0.4	X	Test word 0
0.4	X	13±1	13±1	2.4	X	Test word 1
0.4	X	13±1	X	X	X	All LOW

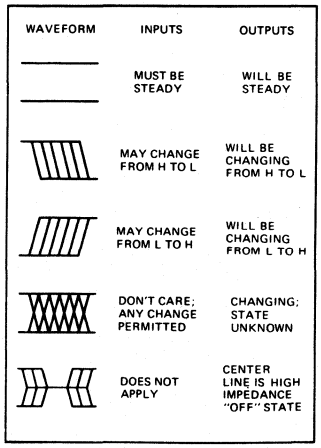
X = Don't Care (0 - 5V)

Note: 13V supply should be current limited with 300 ohm resistors.

Programming boards are available for the Data I/O automatic programmer. Order part no. 909–1119–1 for the two board set.

SWITCHING CHARACTERISTICS



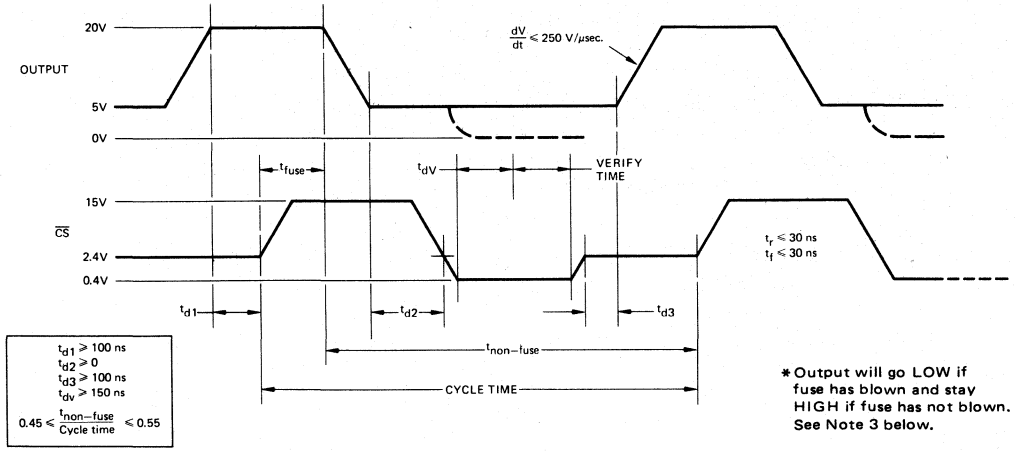


Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

PROGRAMMING REQUIREMENTS

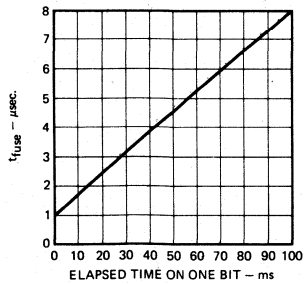
Parameter	Description	Min.	Max.	Units
V_{OP}	Voltage On Output to be Programmed	19.5	20.5	V
V_{ONP}	Voltage on Output not to be Programmed		V_{CC} +0.3	V
I_{ONP}	Current into Output not to be Programmed		20	mA
dv/dt	Rate of Voltage Change on Output		250	V/μs
V_{CSP}	Voltage on $\overline{CS}$ During Programming	14.5	15.5	V
V_{CSE}	Voltage on $\overline{CS}$ to Verify Chip		0.45	V
V_{CSD}	Voltage on $\overline{CS}$ to Disable Chip	2.4	5.5	V
V_{CCP}	V_{CC} During Programming	5.0	5.5	V
V_{ILP}	Address Input LOW Level		0.45	V
V_{IHP}	Address Input HIGH Level	2.4		V
t_{fuse}	Fusing Pulse Width	1.0	8.0	μs
t_{d1}	Delay Output = 20V to $\overline{CS}$ > 5.5V	100		ns
t_{d2}	Delay Output = 5V to $\overline{CS} \leq$ 2.4V	0		ns
t_{dv}	Delay from $\overline{CS} \leq$ 0.45 V to Verify	150		ns
t_{d3}	Delay $\overline{CS} \geq$ 2.4V to Output > 5.5V	100		ns
Duty Cycle	Ratio of $\overline{CS} \leq$ 5.5V to Total Period	45	55	%
t_{bit}	Elapsed Time Programming One Bit	0.1	100	ms
t_{cont}	Total Time Power Applied to Device During Programming		1.6	sec
t_{xtra}	Time Programming Pulses are Applied After Blown Fuse is Detected	100		μs

FUSING REQUIREMENTS



Notes:
1. Do not exceed 100ms accumulated programming time on one bit.
2. After 1.6 seconds accumulated programming time, turn all power off for 300ms, then fuse for 200ms, then power off for 300ms, and so on.
3. Continue fusing pulses for 100μs AFTER detecting open fuse.

Fuse Time Versus Time Attempting To Program One Bit



OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor. The program data may be submitted in the form of a truth table, but punched paper tapes are preferrable since they can be handled automatically. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. Your distributor can also supply you with mark-sense cards on which pencil marks are used to indicate program data.

Paper tapes in the ASCII format below are usually the easiest way to specify the program. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1) A leader of at least 25 rubouts.
2) The data patterns for all 32 words, starting with word 0, in the following format:
   a) Any characters, including carriage return and line feed, except "B".
   b) The letter "B", indicating the beginning of the data word.
   c) A sequence of eight Ps or Ns, starting with output O_7.
   d) The letter "F", indicating the finish of the data word.
   e) Any text, including carriage return and line feed, except the letter "B".
3) A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.
When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

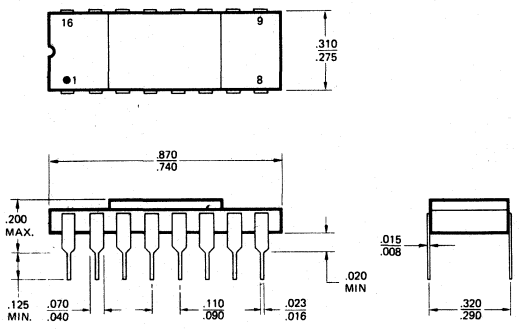
ØØØ	BPNPPNNNPF	WORD ZERO (R) (L)
	BPPPPPPNNF	COMMENT FIELD (R) (L)
ØØ2	BNNNPPPPNF	ANY (R) (L)
	BNNNNNNNNF	TEXT (R) (L)
ØØ4	BPNNNNNNPF	CAN (R) (L)
	BNPPNPPNNF	GO (R) (L)
ØØ6	BPNNPPPNNF	HERE (R) (L)
•	•	•
•	•	•
Ø31	BNNNNPPPNF	END (R) (L)

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	H	H	L	H	L	L	H	H	H	L	L
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H	H	H	H	H	L	L	L	L	H	H	H	L

PHYSICAL DIMENSIONS
Dual-In-Line



Am29760 • Am29761

256-Word by 4-Bit PROM's

Distinctive Characteristics

- Field programmable read only memory
- Highly reliable polysilicon fuses
- Pin compatible with other popular 256 by 4 PROMS
- Typical fusing time of 200μs/bit
- 60ns access time at 25°C
- Three-state and open-collector versions

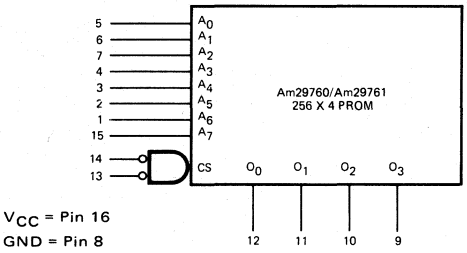
FUNCTIONAL DESCRIPTION

The Am29760 and Am29761 are electrically programmable Low-Power Schottky TTL read only memories. Both devices are organized as 256 words of 4 bits each; the Am29760 has open collector outputs and the Am29761 has three-state outputs. The devices are shipped with all bits HIGH and each bit in the memory can be programmed to a LOW by applying appropriate voltages to the circuit. At each bit location on the circuit there is a narrow link of polysilicon material which is conductive, but which can be opened like a fuse by passing a short, high-current pulse through it. The fusing process simply melts the polysilicon at the center of the link and the two melted ends pull away from each other insuring a very reliable open circuit, which produces a LOW at the memory output.

The programming voltage is applied at the output pin for the bit to be programmed, while the word to be programmed is selected by normal TTL levels on the address lines. The passage of current through the link is controlled by a programming pulse on the chip select input. There are two extra words and one additional bit for each word on the chip which are programmed at the factory during testing to insure high programming yields in devices shipped.

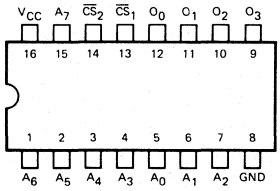
After programming, the device can be used for microprogram storage or random logic function generation, like any read-only memory. If either chip select input is held HIGH, the outputs will all turn off, so the outputs of several memories can be tied together for expansion.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
Top View

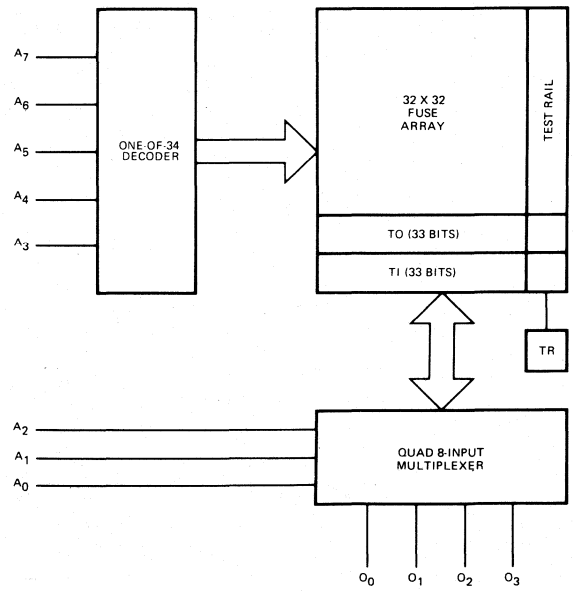


Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM29760DC
Hermetic DIP	−55°C to +125°C	AM29760DM
Hermetic Flat Pak	−55°C to +125°C	AM29760FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM29761DC
Hermetic DIP	−55°C to +125°C	AM29761DM
Hermetic Flat Pak	−55°C to +125°C	AM29761FM

BLOCK DIAGRAM



TO = Test Word
TI = Test Word
TR = Test Rail

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Input Voltage (Address Inputs)	−0.5V to +5.5V
DC Voltage Applied to Outputs During Programming	25V
Output Current into Outputs During Programming	125 mA
DC Input Voltage (Chip Select Input — Pin 13)	−0.5V to +15.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

Am29760XC, Am29761XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%	COM'L
Am29760XM, Am29761XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%	MIL

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am29761 Only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA			0.4	Volts
			I_{OL} = 16mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V			−0.010	−0.100	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				10	µA
I_I	Input HIGH current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC} (Am29761 Only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)		−12	−35	−85	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.			55	80	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	V
I_{CEX}	Output Leakage Current	V_{CC} = MAX V_{CS} = 2.4V	V_O = 4.5V			100	µA
			V_O = 2.4V			40	
			V_O = 0.4V			−40	

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

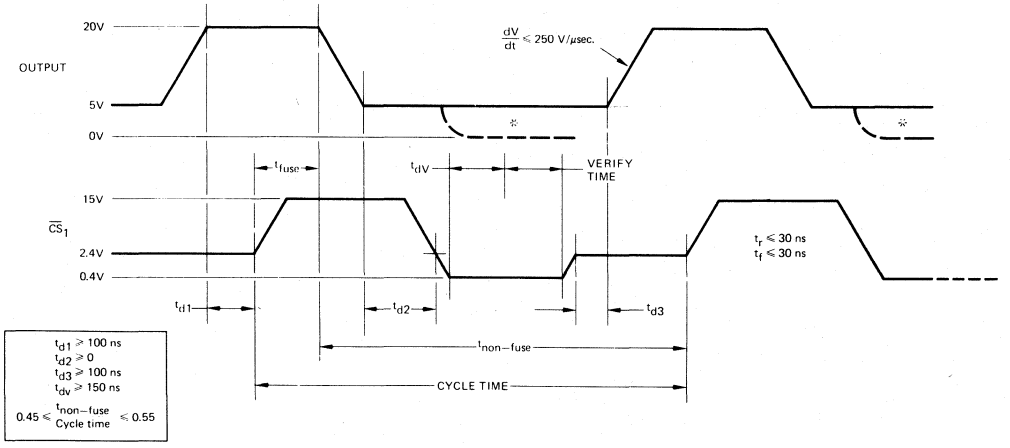
Parameter	Description	Test Conditions	Typ. 5V 25°C	Max. 25°C	Max. Com'l	Max. Mil	Units
t_{AA}	Address Access Time	C_L = 30 pF R_L = 300 Ω to V_{CC} and 600 Ω to GND (16 mA Load) Note 1	45	60	70	80	ns
t_{EA}	Enable Access Time		25	30	35	40	ns
t_{ER}	Enable Recovery Time		25	30	35	40	ns

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

PROGRAMMING REQUIREMENTS

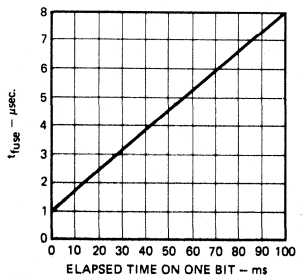
Parameter	Description	Min.	Max.	Units
V_{OP}	Voltage On Output to be Programmed	19.5	20.5	V
V_{ONP}	Voltage on Output not to be Programmed		V_{CC} +0.3	V
I_{ONP}	Current into Output not to be Programmed		20	mA
dv/dt	Rate of Voltage Change on Output		250	V/μs
V_{CSP}	Voltage on $\overline{CS}1$ During Programming	14.5	15.5	V
V_{CSE}	Voltage on $\overline{CS}1$ to Verify Chip		0.45	V
V_{CSD}	Voltage on $\overline{CS}1$ to Disable Chip	2.4	5.5	V
V_{CCP}	V_{CC} During Programming	5.0	5.5	V
V_{ILP}	Address Input LOW Level		0.45	V
V_{IHP}	Address Input HIGH Level	2.4		V
t_{fuse}	Fusing Pulse Width	1.0	8.0	μs
t_{d1}	Delay Output = 20V to $\overline{CS}$ > 5.5V	100		ns
t_{d2}	Delay Output = 5V to $\overline{CS} \leq$ 2.4V	0		ns
t_{dv}	Delay from $\overline{CS} \leq$ 0.45 V to Verify	150		ns
t_{d3}	Delay $\overline{CS} \geq$ 2.4V to Output > 5.5V	100		ns
Duty Cycle	Ratio of $\overline{CS} \leq$ 5.5V to Total Period	45	55	%
t_{bit}	Elapsed Time Programming One Bit	0.1	400	ms
t_{cont}	Total Time Power Applied to Device During Programming		1.6	sec
t_{xtra}	Time Programming Pulses are Applied After Blown Fuse is Detected	100		μs

FUSING REQUIREMENTS



Notes:
1. Do not exceed 400ms accumulated programming time on one bit.
2. After 1.6 seconds accumulated programming time turn all power off for 600ms, then fuse for 400ms, then power off for 600ms, and so on.
3. Continue fusing pulses for 100μs AFTER detecting open fuse.
4. Hold CS_2 (Pin14) LOW during programming.

Fuse Time Versus Time Attempting To Program One Bit



PROGRAMMING THE Am29760 AND Am29761

The Am29760 and Am29761 are shipped with a polysilicon fusible link at each bit location. The output of the memory with the link in place is HIGH. To program the device the fusible links are selectively opened; reading an open location produces a LOW at the memory output.

The link is opened by passing a large current through it from a voltage supply of 20 V on the memory output. The current is directed through the fuse by raising the $\overline{CS}1$ input to 15 volts. After a short programming pulse, the 20-volt supply is removed, the chip is enabled, and the output level is sensed to determine whether or not the link has opened. If it has not opened another programming sequence is initiated on the output and chip select lines. If the link has opened — that is, a LOW is sensed — the programming pulses are continued for 100 μsec to insure that the bit has been programmed reliably.

Most links will open with a few one microsecond programming pulses. Occasionally a link will be a little stronger and will require a longer programming pulse. The duration of the programming pulse may be gradually lengthened up to 8 μsec until a total elapsed time of 400msec has been spent on one bit. A link which has not opened by 400ms is most likely defective, and further programming of the device should not be attempted.

The memories will become hot during the programming due to the large currents being passed. Programming pulses should not be applied to one device more than 1.6 seconds to avoid heat damage. If this programming time is ever exceeded, all power to the chip, including V_{CC}, should be removed for a period of 600ms, after which programming can continue in cycles of 400ms programming and 600ms power off.

TEST WORDS

The Am29760 and Am29761 have an extra bit on each word in the fuse matrix, and two extra words, making the matrix 33 bits by 34 words. The test rail is accessible only on the die and cannot be examined on packaged units. The two test words can be accessed by applying special voltages to the A_6 and A_7 address inputs. The select code on A_0-A_2 determines which 4 of 32 bits in the test word are connected to the output. These words are programmed at the factory prior to shipment.

There is also a special address condition which forces all memory outputs to the LOW state, allowing verification of output LOW characteristics prior to programming.

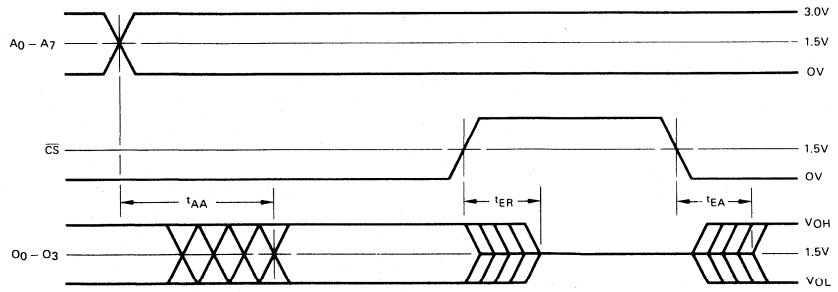
INPUTS (Volts)							OUTPUTS
$\overline{CS}$	A_7	A_6	A_5	A_4	A_3	A_2-A_0	$O_3 - O_0$
0.4	13.0	13.0	X	X	0.4	Select	Test word 0
0.4	13.0	13.0	X	X	2.4	Select	Test word 1
0.4	13.0	X	X	X	X	X	All LOW

X = Don't Care (0 — 5V)

Note: 13V supply should be current limited with 300 ohm resistors.

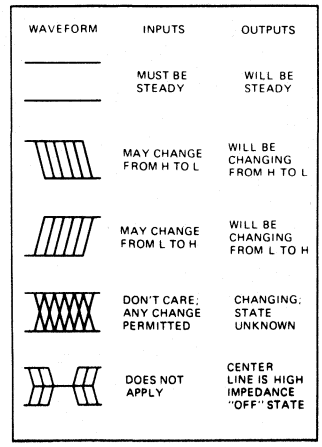
Programming boards are available for the Data I/O automatic programmer. Order part no. 1176-1

SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

KEY TO TIMING DIAGRAM



OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor. The program data may be submitted in the form of a truth table, but punched paper tapes are preferrable since they can be handled automatically. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. Your distributor can also supply you with mark-sense cards on which pencil marks are used to indicate program data.

Paper tapes in the ASCII format below are usually the easiest way to specify the program. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1) A leader of at least 25 rubouts.
2) The data patterns for all 256 words, starting with word 0, in the following format:
   a) Any characters, including carriage return and line feed, except "B".
   b) The letter "B", indicating the beginning of the data word.
   c) A sequence of four Ps or Ns, starting with output O_3.
   d) The letter "F", indicating the finish of the data word.
   e) Any text, including carriage return and line feed, except the letter "B"
3) A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

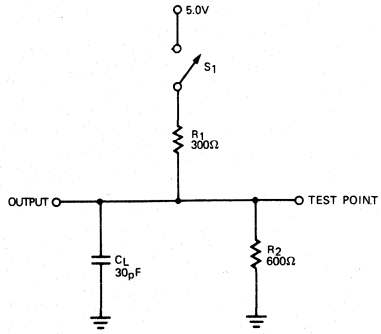
TYPICAL PAPER TAPE FORMAT

ØØØ	BNNNPF	WORD ZERO (R) (L)
	BPPNNF	COMMENT FIELD (R) (L)
ØØ2	BPPPNF	ANY (R) (L)
	BNNNNF	TEXT (R) (L)
ØØ4	BNNNPF	CAN (R) (L)
	BPPNNF	GO (R) (L)
ØØ6	BPPNNF	HERE (R) (L)
⋮	⋮⋮⋮⋮⋮⋮	⋮
255	BPPPNF	END (R) (L)

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

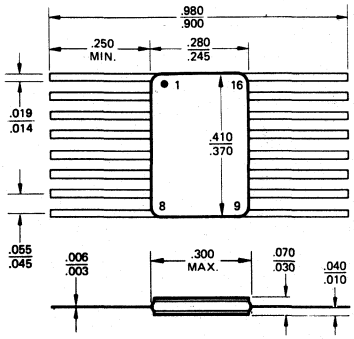
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	H	H	L	H	H	L	L
				⋮					⋮		
H	H	H	H	H	H	H	H	H	H	H	L

AC TEST CIRCUIT

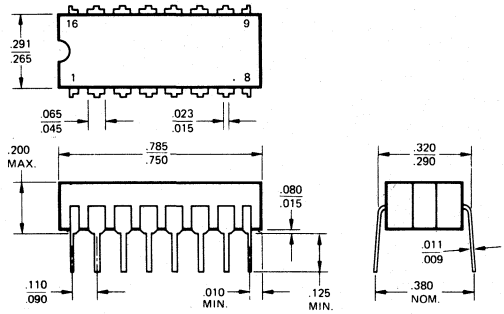


PHYSICAL DIMENSIONS
Dual-In-Line

16-Pin Flat Pack



Ceramic



Am29790 • Am29791

Field Programmable Logic Array

PRELIMINARY DATA

Distinctive Characteristics

- LSI replacement for random logic and inefficiently used ROMs and PROMs
- 16 inputs — 8 outputs — 48 product terms
- Logic equation for each output field programmed by fusing polysilicon links
- Each output can be programmed to be active HIGH or active LOW
- 100% processing in accordance with MIL-STD-883
- Three-state or open collector outputs controlled by active LOW chip enable.

ORDERING INFORMATION

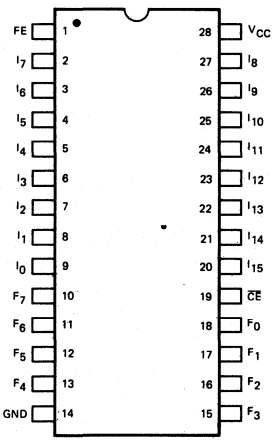
This data is based on design goals and is subject to change following complete characterization.

FUNCTIONAL DESCRIPTION

The Am29790 and Am29791 are field programmable random logic arrays. The Am29791 has three-state outputs and the Am29790 has open collector outputs. The devices have 16 data inputs and contain 48 intermediate product terms. Random logic functions are implemented by using the device like 8 large AND-OR-INVERT gates. Up to 48 AND functions may be generated in the device, where each AND function is the product of any or all of the 16 inputs (I_0-I_{15}) or their complements. Any of the AND functions which have been generated may then be OR'ed to form an output function on one of the F outputs. The F output may also be programmed to invert, i.e., form an AND-OR-INVERT function, rather than AND-OR.

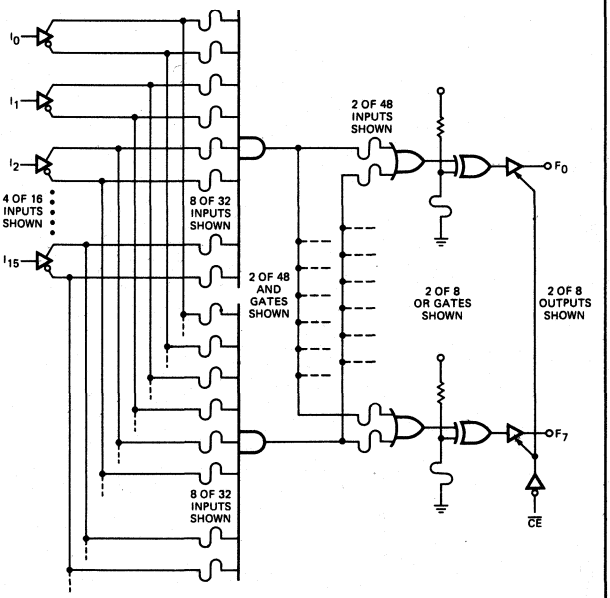
Units are shipped with all fuses intact, and all outputs LOW. Each of the 48 AND functions contains both true and complement of each of the 16 input variables. (Therefore all AND functions are initially false). A variable (or its complement) is inserted into an AND gate by blowing the fuse for the undesired state. A variable is removed from an AND gate by blowing both the true and complement fuses. Each OR function contains the outputs of all 48 AND functions. AND functions are removed from the OR gates by blowing the proper fuse. If the output is to be negated, then a fuse is blown on an EXCLUSIVE-OR gate at the output. That output then becomes an AND-OR-INVERT function of the inputs. The chip enable input ($\overline{CE}$) forces all outputs OFF when HIGH. When LOW, the outputs will be OFF or LOW for the Am29790, or HIGH or LOW for the Am29791.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC BLOCK DIAGRAM



OPERATING RANGE

Part No.	Ambient Temperature	V_{CC}
Am29790DC, Am29791DC	T_A = 0°C to +75°C	5.0V ±5%
Am29790DM, Am29791DM	T_A = −55°C to +125°C	5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am29791 Only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 12mA V_{IN} = V_{IH} or V_{IL}			0.3	0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V			−0.03	−0.25	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V			<1	25	μA
I_{SC} (Am29791 Only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−12	−35	−90	mA
I_{CC}	Power Supply Current	$\overline{CE}$ = GND, all other inputs = 4.5V V_{CC} = MAX.			120		mA
V_C	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{CEX}, I_{OLK}	Output Leakage Current	$V_{\overline{CE}}$ = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.45V	−40			

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			Am29790DC Am29791DC			Am29790DM Am29791DM			
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
$t_{PZL}(\overline{CE})$ $t_{PZH}(\overline{CE})$	Delay Chip Select to Output Active HIGH or LOW	C_L = 30pF R_L = 300Ω to V_{CC} and 600Ω to GND (16mA Load) Note 2		25			40		ns
$t_{PLZ}(\overline{CE})$ $t_{PHZ}(\overline{CE})$	Delay Chip Select HIGH to Output OFF			25			40		ns
$t_{PLH}(I)$	Delay Input to Output HIGH			30			50		ns
$t_{PHL}(I)$	Delay Input to Output LOW								

Note 2. 300Ω resistor opened for t_{DIS} and t_{EN} measurements between HIGH and OFF states.

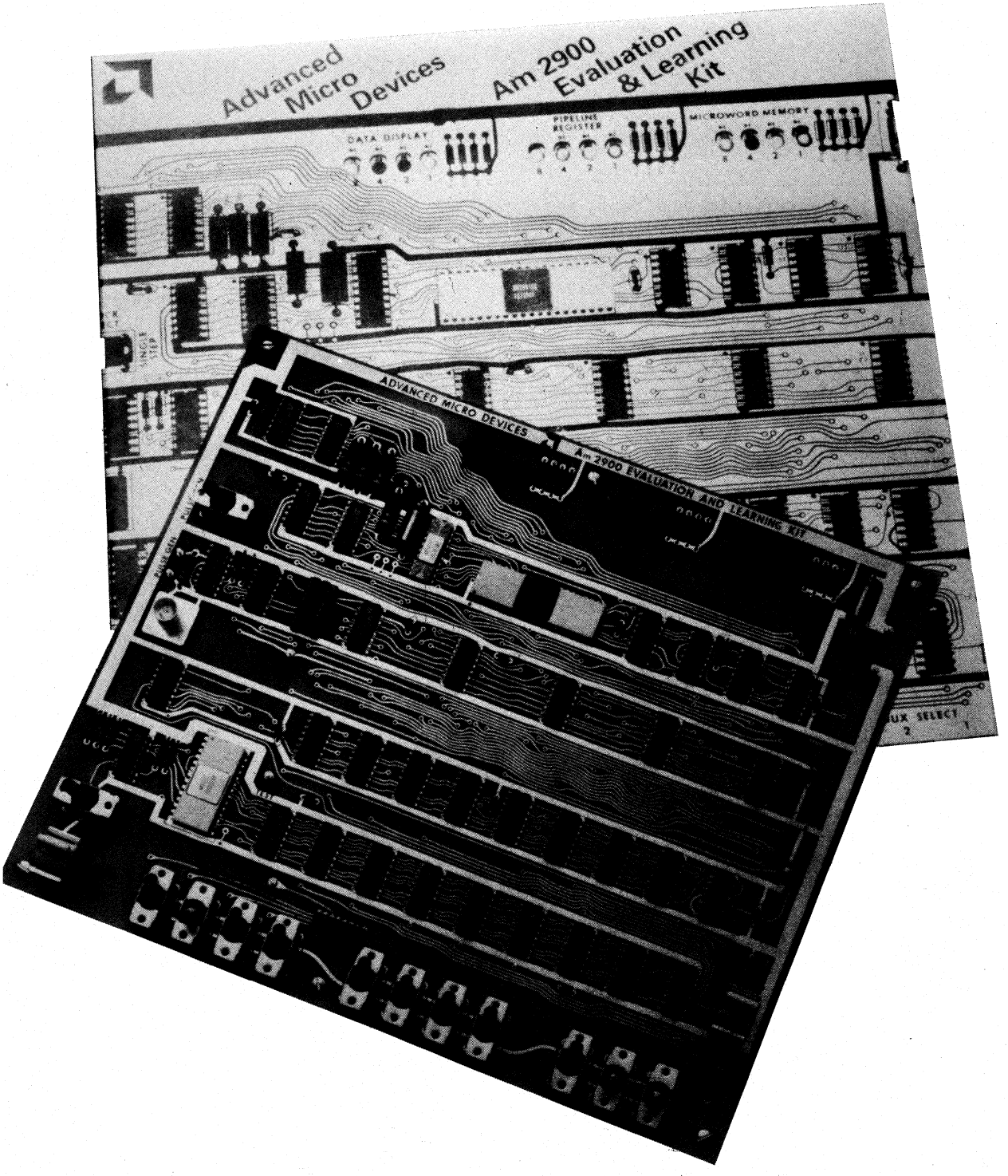
PROGRAMMING PROCEDURE

Programming is facilitated by two internal 1-of-48 decoders used to select one of the 48 product terms. One of these decoders is activated by applying high-voltage logic to inputs I_0-I_5, and the other by applying high voltage logic to outputs F_0-F_5.

Input variables which are not desired in a particular AND gate are fused out by selecting the AND gate with the decoder on output F_0-F_5, applying a HIGH or LOW TTL level to the input variable to be fused, applying high voltage levels to all other input variables, and pulsing the chip enable input.

Product terms which are to be removed from an OR gate are fused out by selecting the appropriate AND gate using the decoder on inputs I_0-I_5, applying a high voltage level to the output for the desired OR gate, and pulsing the chip enable input.

The polarity of the output may be inverted by deselecting the chip, applying a high voltage to the desired output, and pulsing the FE input.


Advanced Micro Devices
Am 2900 Evaluation & Learning Kit
DATA DISPLAY
PIPELINE REGISTER
MICROWORD MEMORY
ADVANCED MICRO DEVICES
Am 2900 EVALUATION AND LEARNING KIT

THE Am2900 EVALUATION AND LEARNING KIT

Pictured at the left is the Am2900 Evaluation Kit. The system consists of a microprogrammed control unit which controls all the inputs to an Am2901 microprocessor slice. Thirty-two bit microinstructions are entered into a RAM in the control unit using the switch register. Each microinstruction contains bits to control the Am2901's A and B addresses, instruction, carry in, and data input. Additional bits in the microinstruction control an Am2909 sequencer which generates the addresses for the microprogram memory. Once entered, microinstructions may be executed using a single step clock or using a pulse generator. The LED display provides access to nearly every signal path in the system.

Sixteen "sequence control" instructions are available, including execute, branch conditional, jump-to-subroutine, return, and loop. Because the set of sequence instructions is implemented in a PROM, the user can devise his own set of operations by programming a new PROM.

The kit is supplied with 40 IC's, all resistors, capacitors, LED's and switches, the PC board, and a manual containing assembly instructions, theory and a set of exercises. The user need only solder the components in place and attach a 5V power supply (2.0 ampere rating).

Working with the kit, the user will gain familiarity with a high performance pipelined microprogrammed architecture, and with the operation of the Am2909 and Am2901. By driving the kit from a pulse generator, the user can observe the operation of the components in real time, executing real instructions.

The part number for this kit is Am2900K1.

ADVANCED LOW-POWER SCHOTTKY

ADVANCED SCHOTTKY PROCESSING

Advanced Micro Devices is a major supplier of complex MSI Schottky and Low-Power Schottky integrated circuits. Our book describes over 100 products available in two temperature ranges and three package combinations as well as dice.

Advanced Micro Devices has developed Schottky process technologies and design techniques that optimize the performance capabilities of the circuit functions. An example of the improvements offered by the Advanced Micro Devices Low-Power Schottky process is provided with the comparison below between the Am25LS174 and SN54/74LS174 six-bit registers:

1. Twice the fan-out over the military range (−55°C to 125°C)

   25LS174 I_{OL} = 8mA Max.
   54LS174 I_{OL} = 4mA Max.

2. Higher noise immunity at I_{OL} = 8mA

   25LS174 V_{OL} = 0.45V Max. at 8mA
   74LS174 V_{OL} = 0.50V Max. at 8mA

3. Greater fan-out in the high state

   25LS174 I_{OH} = −440μA
   54/74LS174 I_{OH} = −400μA

4. Higher speed

   25LS174 $f_{MAX.}$ = 40MHz
   54/74LS174 $f_{MAX.}$ = 30MHz

ADVANCED HIGH PERFORMANCE

Based on these improvements, Advanced Micro Devices has introduced complete high performance families of Schottky and Low-Power Schottky logic (Am25 series), interface (Am26 series), memory (Am27 series) and microprocessor (Am29 series) functions. These include both improved performance versions of devices originated by other manufacturers as well as functions originated by Advanced Micro Devices.

A comparison of some improvements offered by the Advanced Micro Devices products over competitive offerings is given below:

- Am25LS MSI logic functions have worst case delays and clock frequencies specified at up to 50% faster for the same or lower power than their SN54/74LS equivalents.
- Am27LS00 256-bit RAM operates at the same speed but only 50% of the power of the 93410A.
- Am2901 4-bit bipolar microprocessor operates at twice the speed and 20% less power than the similar 6701 device. In addition, an extra instruction line provides enhanced logic capability.

An example of improved logic flexibility offered in products originated by Advanced Micro Devices is shown below. The application of Figure 1 shows the use of the Am25LS14 8-bit serial/parallel two's complement multiplier with the Am25LS22 8-bit shift register with sign extend, to implement an 8-bit by 8-bit bus organized multiplier, with 8-bit truncated product, in only two packages.

On the following pages is a selection guide to the Schottky and Low-Power Schottky products manufactured by AMD. Additional information is supplied on some products especially useful in 2900 based systems. For complete information, ask for our Schottky and Low-Power Schottky data book.

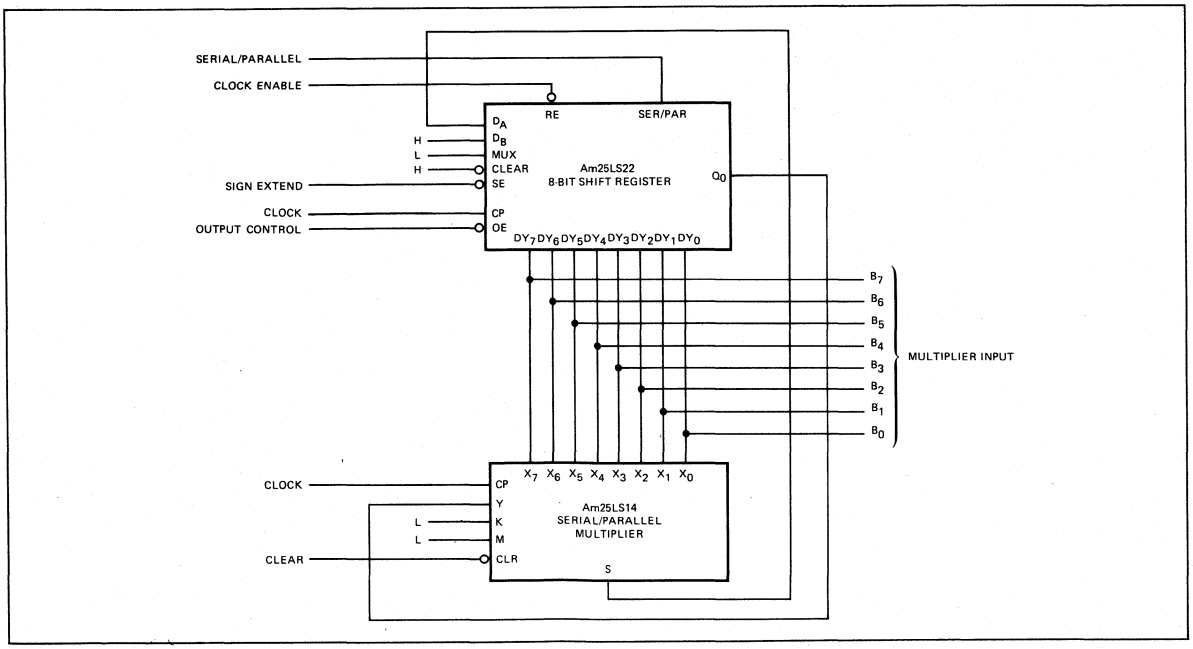


Figure 1. An 8-Bit by 8-Bit Bus Organized Multiplier Using the Am25LS14 and Am25LS22.

FUNCTIONAL INDEX AND SELECTOR GUIDE

This guide divides the AMD Low-Power Schottky and Schottky TTL Product Line by function into three basic performance categories:

1. High-Performance, Low-Power Schottky
   Ex. 25LS174 Six Bit Register. f_{max} = 40 MHz (Min.)
2. Standard Low-Power Schottky
   Ex. 74LS174 Six Bit Register. f_{max} = 30 MHz (Min.)
3. High-Speed Schottky
   Ex. 74S174 Six Bit Register. f_{max} = 75 MHz (Min.)

DESCRIPTION	HIGH-PERFORMANCE LOW-POWER SCHOTTKY	STANDARD LOW-POWER SCHOTTKY	HIGH-SPEED SCHOTTKY
DECADE (BCD) COUNTERS			
Asynchronous Clear	25LS160	54/74LS160	54/74S160
Asynchronous Clear			93S10
Synchronous Clear	25LS162	54/74LS162	
Up-Down, Synchronous Preset	25LS168	54/74LS168	
Up-Down, Asynchronous Preset, Single Clock	25LS190	54/74LS190	
Up-Down, Asynchronous Preset, Dual Clock	25LS192	54/74LS192	
Up-Down, Synchronous Preset, Three-State	25LS2568		
BINARY HEXADECIMAL COUNTERS			
Asynchronous Clear	25LS161	54/74LS161	54/74S161
Asynchronous Clear			93S16
Synchronous Clear	25LS163	54/74LS163	
Up-Down, Synchronous Preset	25LS169	54/74LS169	
Up-Down, Asynchronous Preset, Single Clock	25LS191	54/74LS191	
Up-Down, Asynchronous Preset, Dual Clock	25LS193	54/74LS193	
Up-Down, Synchronous Preset, Three-State	25LS2569		
DECODER/DEMULTIPLEXERS			
One-of-Ten Decoder/Demultiplexer, Polarity Control	25LS2537		
One-of-Eight Decoder/Demultiplexer	25LS138	54/74LS138	54/74S138
Dual One-of-Four Decoder/Demultiplexer	25LS139	54/74LS139	54/74S139
Dual One-of-Four Decoder/Demultiplexer			93S21
One-of-Eight Decoder/Demultiplexer, Polarity Control	*25LS2538		
Dual One-of-Four Decoder/Demultiplexer, Polarity Control	25LS2539		
MULTIPLEXERS			
Eight-Input Multiplexer	25LS151	54/74LS151	54/74S151
Three-State Eight-Input Multiplexer	25LS251	54/74LS251	54/74S251
Dual Four-Input Multiplexer	25LS153	54/74LS153	54/74S153
Three-State Dual Four-Input Multiplexer	25LS253	54/74LS253	54/74S253
Quad Two-Input Multiplexer; Non-Inverting	25LS157	54/74LS157	54/74S157
Quad Two-Input Multiplexer; Non-Inverting			93S22
Three-State Quad Two-Input Multiplexer; Non-Inverting	25LS257	54/74LS257	54/74S257
Quad Two-Input Multiplexer; Inverting	25LS158	54/74LS158	54/74S158
Three-State Quad Two-Input Multiplexer; Inverting	25LS258	54/74LS258	54/74S258
MONOSTABLE (ONE-SHOT)			
Dual Retriggerable, Resettable Monostable Multivibrator			26S02
Dual Regriggerable, Resettable Monostable Multivibrator	25LS123A	54/74LS123A	
OPERATORS (ALU etc.)			
Four by Two Two's Complement Multiplier			*25S05
Four-Bit, Four-Way Shifter			*25S10
Eight by One Serial/Parallel Two's Complement Multiplier	*25LS14		
Four-Bit ALU/Function Generator	25LS181	54/74LS181	54/74S181
Four-Bit ALU/Function Generator	25LS2517		
Four-Bit ALU/Function Generator	25LS381	54/74LS381	
Four-Bit Parallel Accumulator	25LS281	54/74LS281	
Priority Encoder	25LS148	54/74LS148	
Four-Bit Serial Adder/Subtractor	*25LS15		

*Portion of data sheet included in this book on following pages.

FUNCTIONAL INDEX AND SELECTOR GUIDE (Cont.)

DESCRIPTION	HIGH PERFORMANCE LOW-POWER SCHOTTKY	STANDARD LOW-POWER SCHOTTKY	HIGH-SPEED SCHOTTKY
PARITY CHECKER/GENERATORS			
Nine-Input Parity Checker/Generator			*82S62
Twelve-Input Parity Checker/Generator			93S48
REGISTERS			
Four-Bit Register with Common Clock Enable	*25LS08	54/74LS379	25S08
Four-Bit Register with Two-Input Multiplexer on Inputs	*25LS09	54/74LS399	25S09
Four-Bit Register with Standard and Three-State Outputs	25LS2518		25S18
Four-Bit Register with Standard and Three-State Outputs			2918
Quad Register with Common Clear	25LS175	54/74LS175	54/74S175
Four-Bit Register; Shift Right, Left or Parallel Load	25LS194A	54/74LS194A	54/74S194
Four-Bit Register; Shift Right or Parallel Load	25LS195A	54/74LS195A	54/74S195
Six-Bit Register with Common Clock Enable	*25LS07	54/74LS378	25S07
Six-Bit Register with Common Clear	25LS174	54/74LS174	54/74S174
Eight-Bit, Serial-In, Parallel-Out Shift Register	25LS164	54/74LS164	
Eight-Bit Shift/Storage Register; Synchronous Clear	*25LS23		
Eight-Bit Shift/Storage Register; Asynchronous Clear	25LS299	54/74LS299	
Eight-Bit Shift/Storage Register with Sign Extend	*25LS22		
Octal D-Type Register, Common Clear	25LS273	54/74LS273	
Octal D-Type Register (Three-State)	25LS374	54/74LS374	
Octal D-Type Register, Common Enable	25LS377	54/74LS377	
Octal D-Type Register, Common Enable and Clear, Three-State	25LS2520		
Quad Two-Output Three-State Register	25LS2526		
BUS TRANSCEIVERS			
Quad Bus Transceiver, Inverting			*26S10
Quad Bus Transceiver, Non-Inverting			*26S11
Quad Open-Collector Bus Transceiver			26S12/12A
Quad Three-State Bus Transceiver			*8T26
Octal Bus Driver, Inverting	25LS240A		54/74S240
Octal Bus Driver, Non-Inverting	25LS241A		54/74S241
Octal Bus Driver, Inverting	25LS2540		
Octal Bus Driver, Non-Inverting	25LS2541		

*Portion of data sheet included in this book on following pages.

Am25S05

Four-Bit by Two-Bit 2's Complement Multiplier

Distinctive Characteristics

- Provides 2's complement multiplication at high speed without correction.
- Can be used in a combinatorial array or in a time sequenced mode.
- Multiplies two 12-bit signed numbers in typically 115ns.
- Multiplies in active HIGH (positive logic) or active LOW (negative logic) representations.
- Reduced input loading as compared to Am2505.
- 100% reliability assurance testing in compliance with MIL-STD-883.

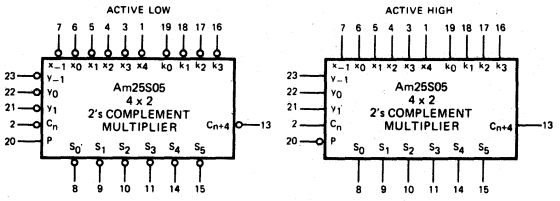
FUNCTIONAL DESCRIPTION

The Am25S05 is a high-speed digital multiplier that can multiply numbers represented in the 2's complement notation and produce a 2's complement product without correction. The device consists of a 4x2 multiplier that can be connected to form iterative arrays able to multiply numbers either directly, or in a time sequenced arrangement. The device assumes that the most significant digit in a word carries a negative weight, and can therefore be used in arrays where the multiplicand and multiplier have different word lengths. The multiplier uses the quaternary algorithm and performs the function S = XY + K where K is the input field used to add partial products generated in the array. At the beginning of the array the K inputs are available to add a signed constant to the least significant part of the product. Multiplication of an m bit number by an n bit number in an array results in a product having m+n bits so that all possible combinations of product are accounted for. If a conventional 2's complement product is required the most significant bit can be ignored, and overflow conditions can be detected by comparing the last two product digits.

A number of connection schemes are possible. Figure 1 shows the connection scheme that results in the fastest multiply. If higher speed is required an array can be split into several parts, and the parts added with high-speed look-ahead carry adders.

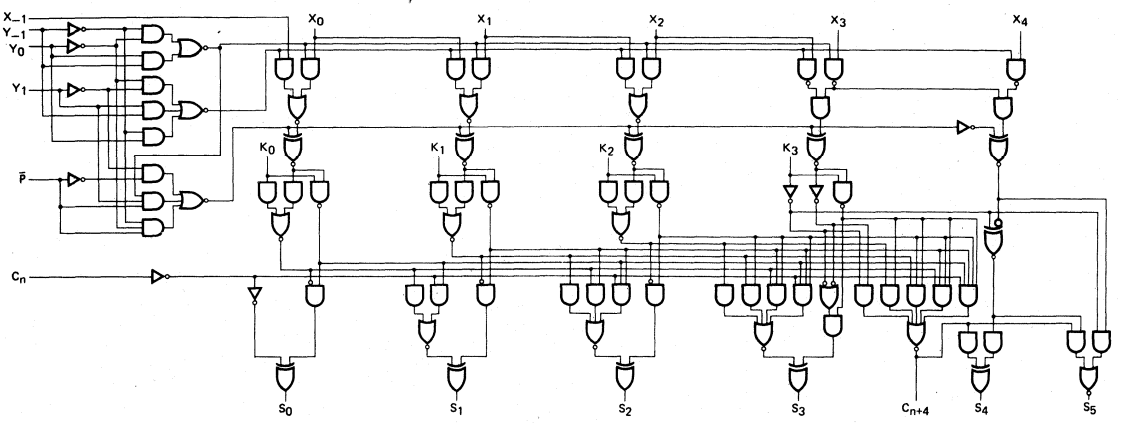
Provision is made in the design for multiplication in the active high (positive logic) or active low (negative logic) representations simply by reinterpreting the active level of the input operands, the product, and a polarity control $\overline{P}$.

LOGIC SYMBOLS



V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM

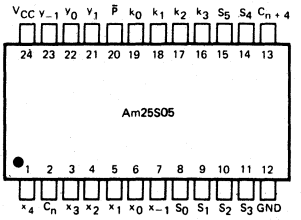


Am25S05 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM25S05PC
Hermetic DIP	0°C to +75°C	AM25S05DC
Dice	0°C to +75°C	AM25S05XC
Hermetic DIP	−55°C to +125°C	AM25S05DM
Hermetic Flat Pak	−55°C to +125°C	AM25S05FM
Dice	−55°C to +125°C	AM25S05XM

Complete data sheets on the devices that follow and the full family of Advanced Micro Devices' Low-Power Schottky MSI Family can be found in Advanced Micro Devices' Schottky and Low-Power Schottky data book.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Am25LS07•Am25LS08

Hex/Quad Parallel D Registers With Register Enable

Distinctive Characteristics

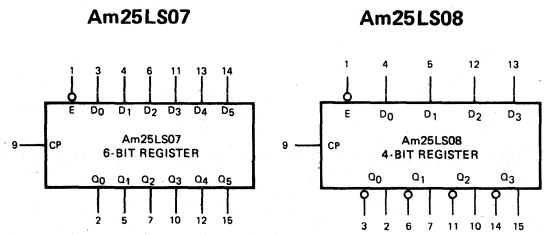
- 4-bit and 6-bit high-speed parallel registers
- Common clock and common enable
- 8mA sink current over full military temperature range
- Positive edge triggered D flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

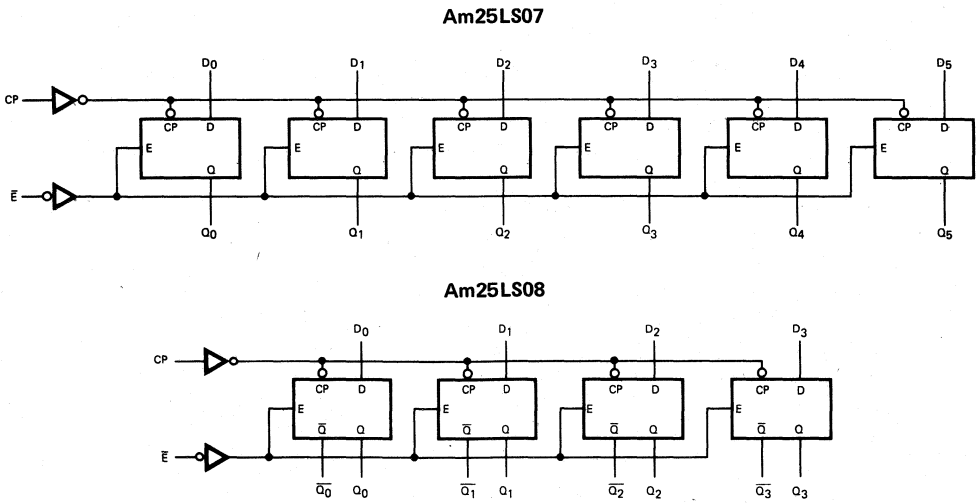
The Am25LS07 is a 6-bit Low Power Schottky register with a buffered common register enable. The Am25LS08 is a 4-bit register with a buffered common register enable. The devices are similar to the Am54LS/74LS174 and Am54LS/74LS175 but feature the common register enable rather than common clear.

Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

LOGIC SYMBOLS



LOGIC DIAGRAMS

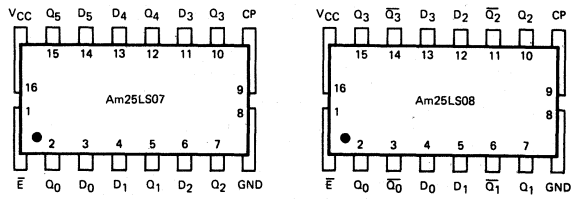


ORDERING INFORMATION

Package Type	Temperature Range	Am25LS07 Order Number	Am25LS08 Order Number
Molded DIP	0°C to +70°C	AM25LS07PC	AM25LS08PC
Hermetic DIP	0°C to +70°C	AM25LS07DC	AM25LS08DC
Dice	0°C to +70°C	AM25LS07XC	AM25LS08XC
Hermetic DIP	−55°C to +125°C	AM25LS07DM	AM25LS08DM
Hermetic Flat Pak	−55°C to +125°C	AM25LS07FM	AM25LS08FM
Dice	−55°C to +125°C	AM25LS07XM	AM25LS08XM

Complete data sheets on the devices that follow and the full family of Advanced Micro Devices' Low-Power Schottky MSI Family can be found in Advanced Micro Devices' Schottky and Low-Power Schottky data book.

CONNECTION DIAGRAMS
Top Views



Note: Pin 1 is marked for orientation.

Am25LS09

Quad Two-Input, High-Speed Register

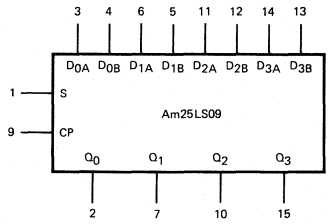
Distinctive Characteristics

- 4-bit register accepts data from one-of-two 4-bit input fields
- Edge triggered clock action
- Advanced low power Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883
- Second source is SN54LS/74LS399
- 8mA sink current over full military temperature range

FUNCTIONAL DESCRIPTION

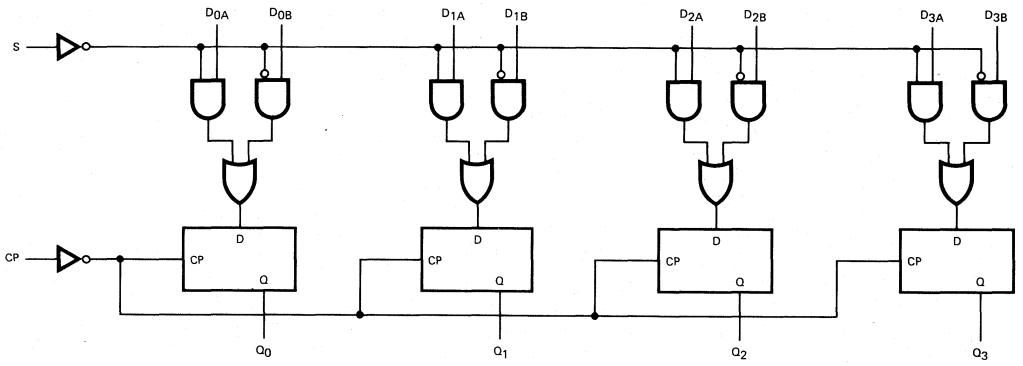
The Am25LS09 is a dual port four-bit register using advanced Low Power Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the D_{iA} input data will be stored in the register. When the S input is HIGH, the D_{iB} input data will be stored in the register.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM

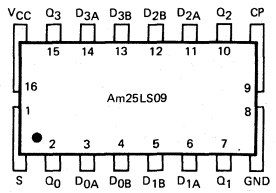


ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS09PC
Hermetic DIP	0°C to +70°C	AM25LS09DC
Dice	0°C to +70°C	AM25LS09XC
Hermetic DIP	-55°C to +125°C	AM25LS09DM
Hermetic Flat Pak	-55°C to +125°C	AM25LS09FM
Dice	-55°C to +125°C	AM25LS09XM

Complete data sheets on the devices that follow and the full family of Advanced Micro Devices' Low-Power Schottky MSI Family can be found in Advanced Micro Devices' Schottky and Low-Power Schottky data book.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Am25S10

Four-Bit Shifter With Three-State Outputs

Distinctive Characteristics

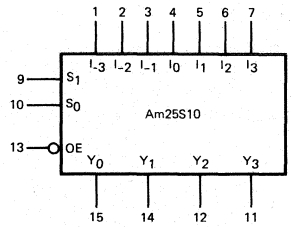
- Shifts 4-bits of data to 0, 1, 2 or 3 places under control of two select lines.
- Three-state outputs for bus organized systems.
- 6.5ns typical data propagation delay.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am25S10 is a combinatorial logic circuit that accepts a four-bit data word and shifts the word 0, 1, 2 or 3 places. The number of places to be shifted is determined by a two-bit select field S_0 and S_1. An active-LOW enable controls the three-state outputs. This feature allows expansion of shifting over a larger number of places with one delay.

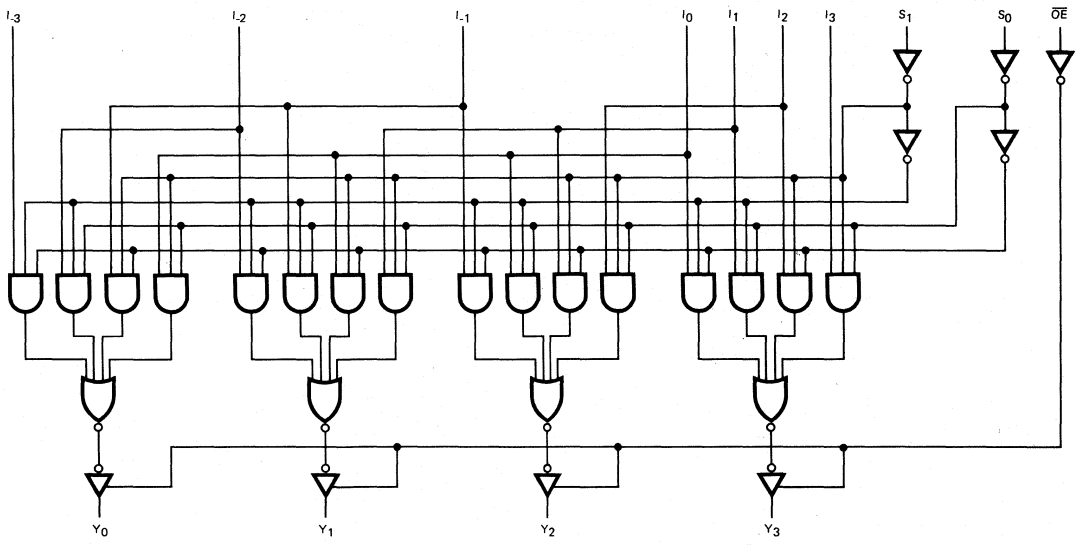
By suitable interconnection, the Am25S10 can be used to shift any number of bits any number of places up or down. Shifting can be logical, with logic zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM

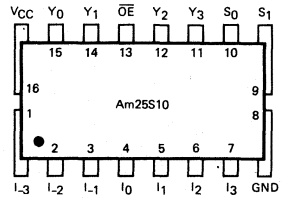


ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25S10PC
Hermetic DIP	0°C to +70°C	AM25S10DC
Dice	0°C to +70°C	AM25S10XC
Hermetic DIP	−55°C to +125°C	AM25S10DM
Hermetic Flat Pak	−55°C to +125°C	AM25S10FM
Dice	−55°C to +125°C	AM25S10XM

Complete data sheets on the devices that follow and the full family of Advanced Micro Devices' Low-Power Schottky MSI Family can be found in Advanced Micro Devices' Schottky and Low-Power Schottky data book.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

Am25LS14

8-Bit Serial/Parallel Two's Complement Multiplier

Distinctive Characteristics

- Two's complement multiplication without correction
- Magnitude only multiplication
- Cascadable for any number of bits
- 8-Bit parallel multiplicand data input
- Serial multiplier data input
- Serial data output for multiplication product
- 25 MHz minimum clock frequency
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

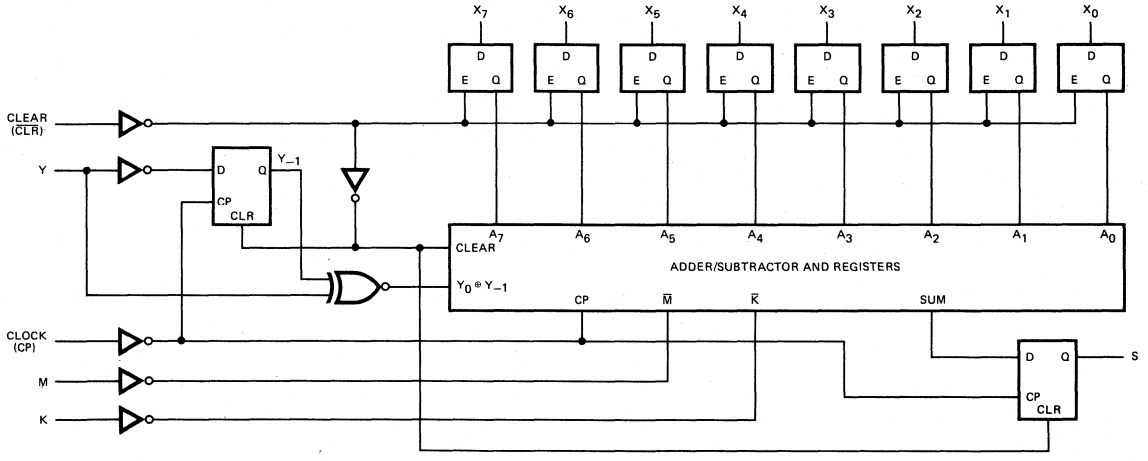
The Am25LS14 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's complement form to produce a two's complement product without correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. The X latches are controlled via the clear input. When the clear input is LOW, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is HIGH, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream—least significant bit first. The product is clocked out the S output least significant bit first.

The multiplication of an m-bit multiplicand by an n-bit multiplier results in an m + n bit product. The Am25LS14 must be clocked for m + n clock cycles to produce this two's complement product. Likewise, the n-bit multiplier (Y-input) sign bit data must be extended for the remaining m-bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The sum (S) output of one device is connected to the K input of the succeeding device when cascading. Likewise, a mode input (M) is used to indicate which device contains the most significant bit. The mode input is wired HIGH or LOW depending on the position of the 8-bit slice in the total X word length.

LOGIC DIAGRAM

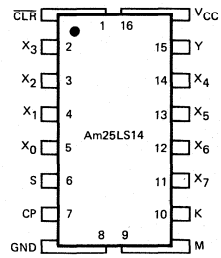


ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS14PC
Hermetic DIP	0°C to +70°C	AM25LS14DC
Dice	0°C to +70°C	AM25LS14XC
Hermetic DIP	–55°C to +125°C	AM25LS14DM
Hermetic Flat Pak	–55°C to +125°C	AM25LS14FM
Dice	–55°C to +125°C	AM25LS14XM

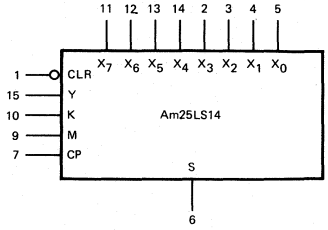
Complete data sheets on the devices that follow and the full family of Advanced Micro Devices' Low-Power Schottky MSI Family can be found in Advanced Micro Devices' Schottky and Low-Power Schottky data book.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

Am25LS15

Quad Serial Adder/Subtractor

Distinctive Characteristics

- Four independent adder/subtractors
- Use with two's complement arithmetic
- Magnitude only addition/subtraction
- Advanced Low Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

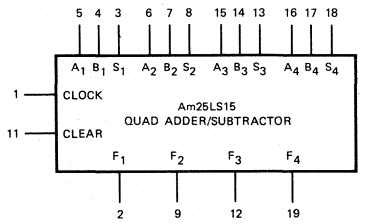
FUNCTIONAL DESCRIPTION

The Am25LS15 is a serial two's complement adder/subtractor designed for use in association with the Am25LS14 serial/parallel two's complement multiplier. This device can also be used for magnitude only or one's complement addition or subtraction.

Four independent adder/subtractors are provided with common clock and clear inputs. The add function is A plus B and the subtract function is A minus B. The clear function sets the internal carry function to logic zero in the add mode and to logic one in subtract mode. This least significant carry is self propagating in the subtract mode as long as zeroes are applied to the A and B inputs at the LSB's. All internal flip-flops change state on the LOW-to-HIGH clock transition.

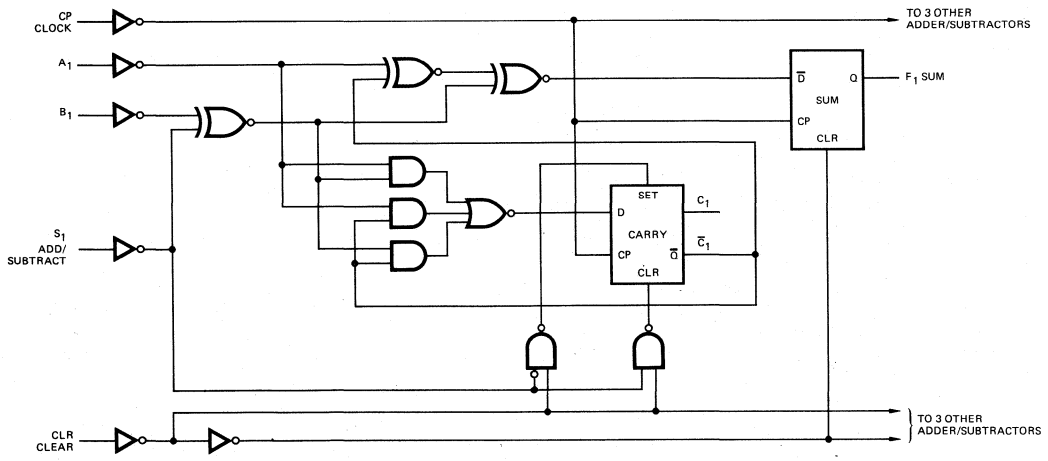
The Am25LS15 is particularly useful for recursive or non-recursive digital filtering or butterfly networks in Fast Fourier Transforms.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM
(One of Four Similar Functions)

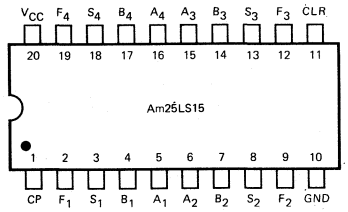


ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS15PC
Hermetic DIP	0°C to +70°C	AM25LS15DC
Dice	0°C to +70°C	AM25LS15XC
Hermetic DIP	–55°C to +125°C	AM25LS15DM
Hermetic Flat Pak	–55°C to +125°C	AM25LS15FM
Dice	–55°C to +125°C	AM25LS15XM

Complete data sheets on the devices that follow and the full family of Advanced Micro Devices' Low-Power Schottky MSI Family can be found in Advanced Micro Devices' Schottky and Low-Power Schottky data book.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Am25LS22

8-Bit Serial/Parallel Register With Sign Extend

Distinctive Characteristics

- Three-state outputs with multiplexed input
- Multiplexed serial data input
- Sign extend function
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

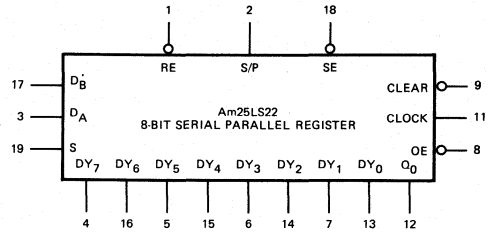
FUNCTIONAL DESCRIPTION

The Am25LS22 is an eight-bit serial/parallel register built using advanced Low-Power Schottky processing. The device features an eight-bit parallel multiplexed input/output port to provide improved bit density in a 20-pin package. Data may also be loaded into the device in a serial manner from either input D_A or D_B. A serial output, Q_0, is also provided.

The Am25LS22 is specifically designed for operation with the Am25LS14 serial/parallel two's complement multiplier and provides the sign extend function required for this device.

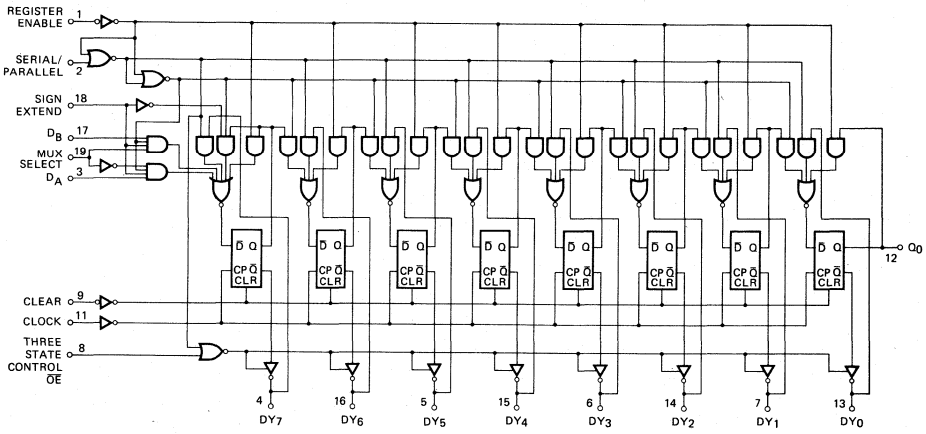
When the Register Enable ($\overline{RE}$) input is HIGH, the register will retain its current contents. Synchronous parallel loading is accomplished by applying a LOW to $\overline{RE}$ and applying a LOW to the Serial/Parallel (S/P) input. This places the three-state outputs in the high-impedance state independent of $\overline{OE}$ and allows data that is applied on the input/output lines (DY_i) to be clocked into the register. When the S/P input is HIGH, the device will shift right. The Sign Extend ($\overline{SE}$) input is used to repeat the sign in the Q_7 flip-flop. This occurs whenever $\overline{SE}$ is LOW when the SHIFT mode is selected. When $\overline{SE}$ is high, the serial two-input multiplexer is enabled. Thus, either D_A or D_B can be selected to load data serially. The register changes state on the LOW-to-HIGH transition of the clock. A clear input (CLR) is used to asynchronously reset all flip-flops when a LOW is applied.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM

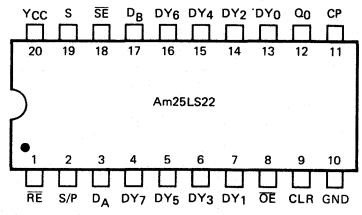


ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS22PC
Hermetic DIP	0°C to +70°C	AM25LS22DC
Dice	0°C to +70°C	AM25LS22XC
Hermetic DIP	−55°C to +125°C	AM25LS22DM
Hermetic Flat Pak	−55°C to +125°C	AM25LS22FM
Dice	−55°C to +125°C	AM25LS22XM

Complete data sheets on the devices that follow and the full family of Advanced Micro Devices' Low-Power Schottky MSI Family can be found in Advanced Micro Devices' Schottky and Low-Power Schottky data book.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Am25LS23

8-Bit Shift/Storage Register with Synchronous Clear

Distinctive Characteristics

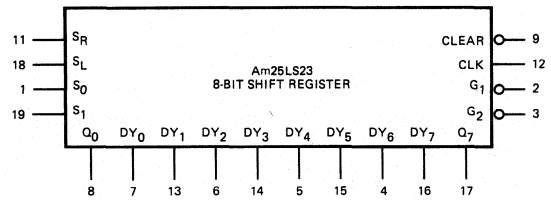
- Synchronous clear
- Three-state outputs
- Common input/output pins
- Cascadable shifting
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am25LS23 is an 8-bit universal shift/storage register with 3-state outputs. The function is similar to the Am25LS299 with the exception of a synchronous clear function. Parallel load inputs and register outputs are multiplexed to allow the use of a 20-pin package. Separate continuous outputs are also provided for flip-flops Q_0 and Q_7.

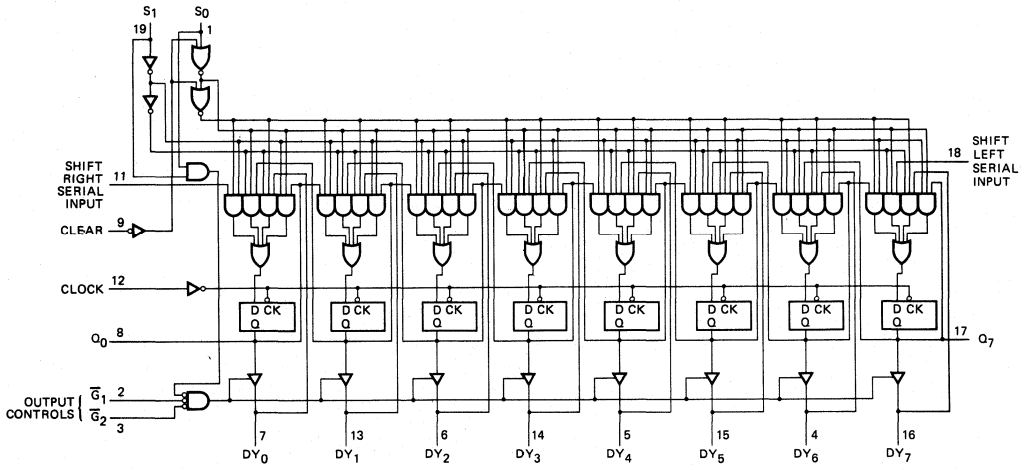
Four modes of operation are possible – Hold (store), Shift-left, Shift-right and Load Data. The Am25LS23 has a typical shift frequency of 50MHz. The Am25LS23 is packaged in a standard 20-pin package.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM

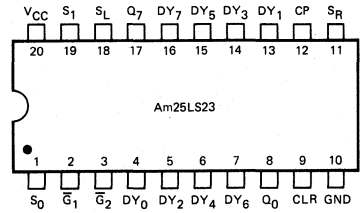


ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS23PC
Hermetic DIP	0°C to +70°C	AM25LS23DC
Dice	0°C to +70°C	AM25LS23XC
Hermetic DIP	–55°C to +125°C	AM25LS23DM
Hermetic Flat Pak	–55°C to +125°C	AM25LS23FM
Dice	–55°C to +125°C	AM25LS23XM

Complete data sheets on the devices that follow and the full family of Advanced Micro Devices' Low-Power Schottky MSI Family can be found in Advanced Micro Devices' Schottky and Low-Power Schottky data book.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Am25LS2538

One-of-Eight Decoder
With Three-State Outputs And Polarity Control

Distinctive Characteristics

- Three-state decoder outputs
- Buffered common output polarity control
- Inverting and non-inverting enable inputs
- Ideal for mask generation, bit manipulation
- Easily cascaded for 16-bit fields

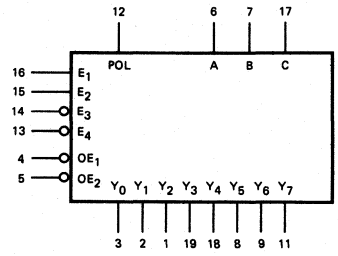
FUNCTIONAL DESCRIPTION

The Am25LS2538 is a three-line to eight-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs — A, B, and C — that are decoded to one-of-eight Y outputs. Two active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

A separate polarity (POL) input can be used to force the function active-HIGH or active-LOW at the output. Two separate active-LOW output enables ($\overline{OE}$) inputs are provided. If either $\overline{OE}$ input is HIGH, the output is in the high impedance (off) state. When the POL input is LOW, the Y outputs are active-HIGH and when the POL input is HIGH, the Y outputs are active-LOW.

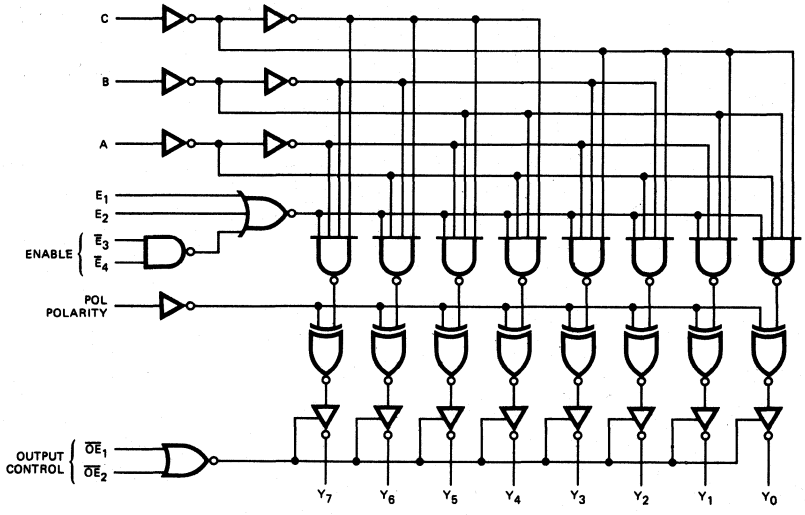
The device is packaged in a space saving (0.3-inch row spacing) 20-pin package. It also features improved switching specifications, higher noise margin, and twice the fan-out over the military temperature range.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM
One-of-Eight Decoder

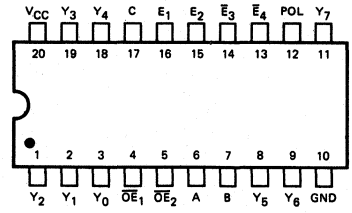


ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS2538PC
Hermetic DIP	0°C to +70°C	AM25LS2538DC
Dice	0°C to +70°C	AM25LS2538XC
Hermetic DIP	–55°C to +125°C	AM25LS2538DM
Hermetic Flat Pak	–55°C to +125°C	AM25LS2538FM
Dice	–55°C to +125°C	AM25LS2538XM

Complete data sheets on the devices that follow and the full family of Advanced Micro Devices' Low-Power Schottky MSI Family can be found in Advanced Micro Devices' Schottky and Low-Power Schottky data book.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Am26S10 / Am26S11

Computer Interface Integrated Circuits

Distinctive Characteristics

- Input to bus is inverting on Am26S10
- Input to bus is non-inverting on Am26S11
- Quad high-speed open collector bus transceivers
- Driver outputs can sink 100mA at 0.8V maximum
- Bus compatible with Am2905, Am2906, Am2907
- Advanced Schottky processing
- PNP inputs to reduce input loading
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am26S10 and Am26S11 are quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.8 volts and four high-speed bus receivers. Each driver output is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving ten Schottky TTL unit loads.

An active LOW enable gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable input can be conveniently driven by active LOW decoders such as the Am25LS139.

The bus output high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 volts.

The Am26S10 and Am26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

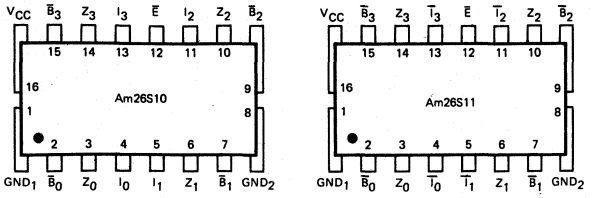
ORDERING INFORMATION

Package Type	Temperature Range	Am26S10 Order Number	Am26S11 Order Number
Molded DIP	0°C to +70°C	AM26S10PC	AM26S11PC
Hermetic DIP	0°C to +70°C	AM26S10DC	AM26S11DC
Dice	0°C to +70°C	AM26S10XC	AM26S11XC
Hermetic DIP	–55°C to +125°C	AM26S10DM	AM26S11DM
Hermetic Flat Pack	–55°C to +125°C	AM26S10FM	AM26S11FM
Dice	–55°C to +125°C	AM26S10XM	AM26S11XM

Complete data sheets on the devices that follow and the full family of Advanced Micro Devices' Low-Power Schottky MSI Family can be found in Advanced Micro Devices' Schottky and Low-Power Schottky data book.

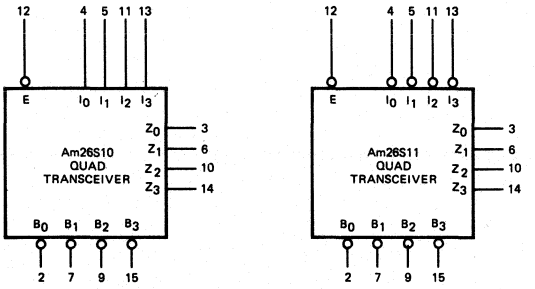
CONNECTION DIAGRAMS

Top Views



Note: Pin 1 is marked for orientation.

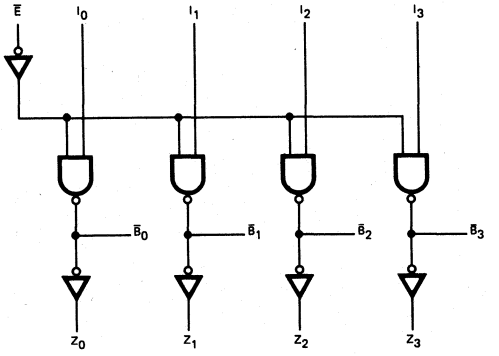
LOGIC SYMBOLS



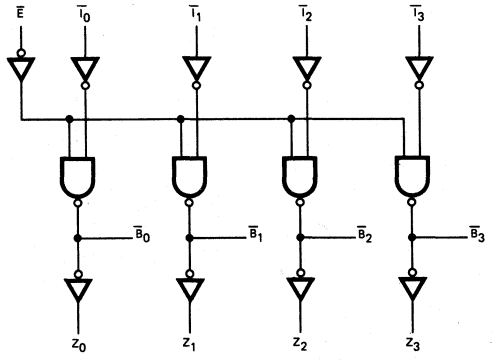
V_{CC} = Pin 16
GND_1 = Pin 1
GND_2 = Pin 8

LOGIC DIAGRAMS

Am26S10



Am26S11



Am8T26/Am8T28

Three-State Quad Bus Transceivers

Distinctive Characteristics

- Advanced Schottky technology
- 40mA driver sink current
- Three-state outputs on driver and receiver
- PNP inputs
- Am8T26 has inverting outputs
- Bus compatible with Am2915, Am2916, Am2917
- 20ns max. driver propagation delay
- 18ns max. receiver propagation delay
- 100% reliability assurance testing in compliance with MIL-STD-883
- Am8T28 has non-inverting outputs

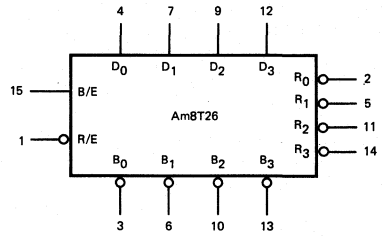
FUNCTIONAL DESCRIPTION

The Am8T26/Am8T28 are high speed bus transceivers consisting of four bus drivers with three-state outputs and four bus receivers, also with three-state outputs. Each driver output is internally connected to a receiver input. Both the drivers and receivers have PNP inputs.

One buffered common "bus enable" input is connected to the four drivers and another buffered common "receiver enable" input is connected to the receivers. A LOW on the bus enable (B/E) input forces the four driver outputs to the high-impedance state. A HIGH on the bus enable allows input data to be transferred onto the data bus.

A HIGH on the receiver enable (R/E) input forces the four receiver outputs to the high-impedance state while a LOW on the receiver enable input allows the received data to be transferred to the output. The complementary design of the bus enable and receiver enable inputs allows these control inputs to be connected together externally such that a single transmit/receive function is derived.

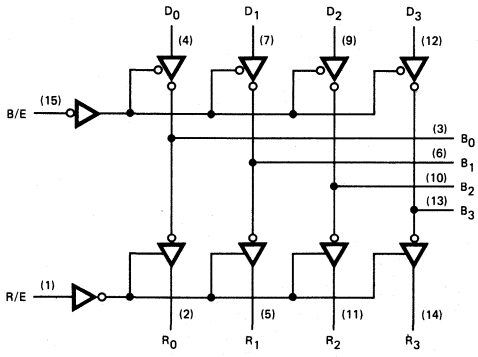
LOGIC SYMBOL



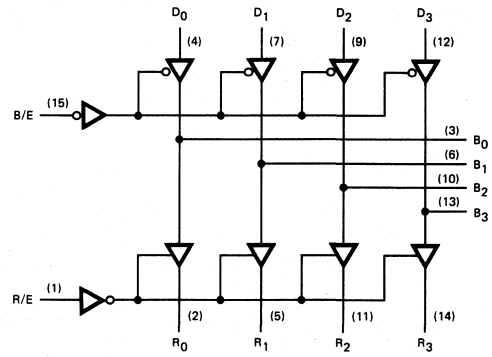
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am8T26
Inverting Output (Three-State)



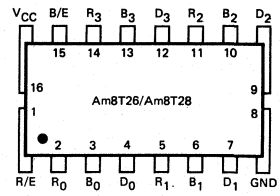
Am8T28
Non-Inverting Output (Three-State)



ORDERING INFORMATION

Package Type	Temperature Range	Am8T26 Order Number	Am8T28 Order Number
Molded DIP	0°C to +75°C	N8T26B	N8T28B
Hermetic DIP	0°C to +75°C	N8T26F	N8T28F
Dice	0°C to +75°C	AM8T26XC	AM8T28XC
Hermetic DIP	−55°C to +125°C	S8T26F	S8T28F
Dice	−55°C to +125°C	AM8T26XM	AM8T28XM

CONNECTION DIAGRAM
(Top View)



Note: Pin 1 is marked for orientation.

Am82S62

Nine-Input Parity Checker/Generator

Distinctive Characteristics

- ODD/EVEN parity outputs
- Inhibit input to disable both outputs
- High-speed expansion input – P_9
- PNP inputs
- Advanced Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883.

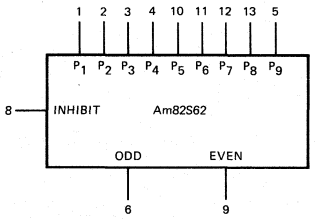
FUNCTIONAL DESCRIPTION

The Am82S62 is a 9-bit parity generator/parity checker with both an ODD parity output and an EVEN parity output. The device can be used to detect errors in data transmission or data retrieval systems as well as to generate this parity check bit.

The Am82S62 features one special high-speed input (P_9) to facilitate expansion. The propagation delay to the outputs through this path is considerably reduced when compared to the P_1 through P_8 paths. This short delay path allows parity checkers/generators of larger size than 9-bits to be built with a minimum of additional delay.

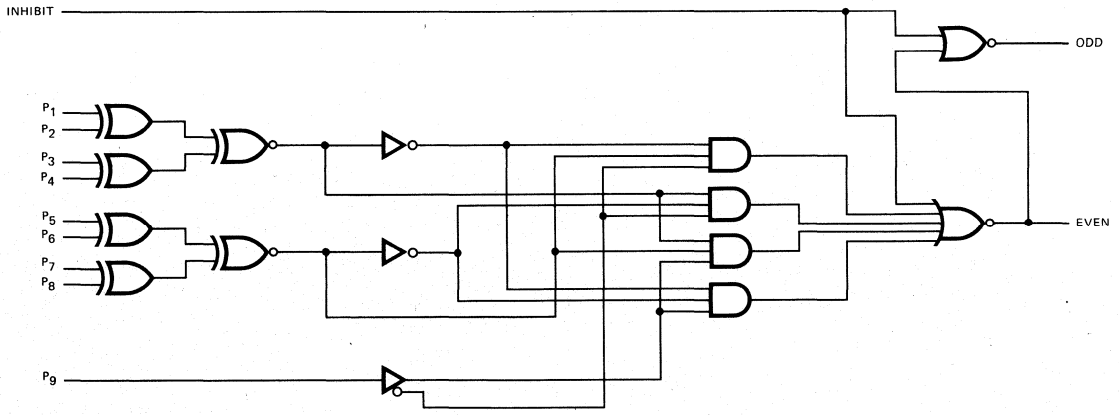
The device is built using advanced Schottky technology and incorporates PNP input transistors to reduce input loading to 0.4 STTL unit loads. The EVEN output is one gate propagation delay time shorter than the ODD output.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM

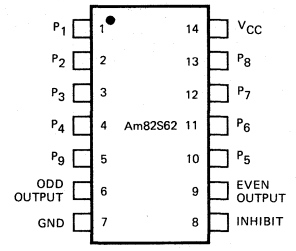


ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	N82S62A
Hermetic DIP	0°C to +75°C	N82S62F
Dice	0°C to +75°C	N82S62X
Hermetic DIP	−55°C to +125°C	S82S62F
Dice	−55°C to +125°C	S82S62X

Complete data sheets on the devices that follow and the full family of Advanced Micro Devices' Low-Power Schottky MSI Family can be found in Advanced Micro Devices' Schottky and Low-Power Schottky data book.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ADVANCED MOS/LSI

Advanced Micro Devices is an industry leader in the production of high-technology MOS products. The company's n-channel, silicon-gate MOS process is ideally suited for the dense, high-speed memory and microprocessor products required by today's systems.

Although most of the MOS products are oriented toward the Am9080A 8-bit MOS microprocessor, the static RAM's are ideal for use with the Am2900 family. The access times of these devices are often well matched to 2900 system microcycle times and provide significant cost benefits over bipolar memories of the same density.

Of particular interest to users of the Am2900 family are the Am9130 and Am9140 4096-bit RAM's. These devices are organized as 4K x 1 and as 1K x 4 and are available with access times to 200ns.

Complete data on these devices is included in the following pages. Also included are brief descriptions of the family of 1K static RAM's, which may be useful in smaller systems. Of course, all these products are available for full military temperature range operation. For complete data on our MOS products, see our MOS/LSI Data Book.

Am9130

1024 x 4 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- 1k x 4 organization
- Fully static data storage — no refreshing
- Single +5V power supply
- High-speed — access times down to 200ns max.
- Low-power — 710mW max. — 350mW typ.
- Interface logic levels identical to TTL
- High noise immunity — 400mV worst case
- High output drive — two standard TTL loads
- Bidirectional data bus — easier system interface
- Dual output controls — flexible bus operations
- Address and data registers on-chip
- Constant power drain — no large surges
- Unique Memory Status signal
  - —improves performance
  - —simplifies timing
- DC standby mode — reduces power by > 80%
- MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DESCRIPTION

The Am9130 products are high performance, low-power, 4096-bit, static, read/write random access memories. They are implemented as 1024 words by 4 bits per word. The data input and output signals are bussed together and share common I/O pins.

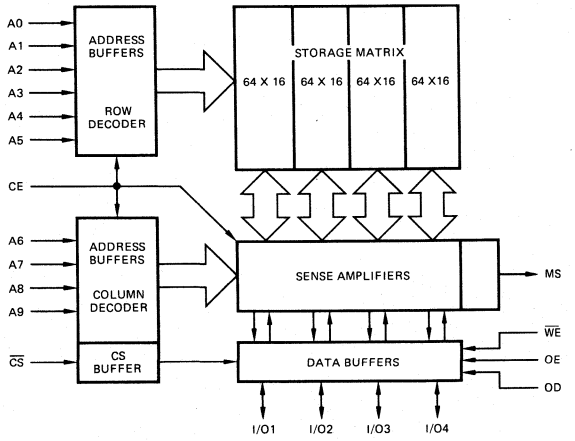
All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. The outputs will drive two full TTL loads or eight LS loads for increased fan-out, better capacitive drive and improved bus interface capability.

Operational cycles are initiated when the Chip Enable signal goes HIGH. When the read or write is complete, Chip Enable goes LOW to prepare the memory for the next cycle. Address and Chip Select signals are latched on-chip to help simplify system timing. Output data is also latched and is available from the access time until into the next operating cycle.

The $\overline{WE}$ signal is HIGH for all read operations and pulsed LOW during the Chip Enable time to perform a write. Memory Status is an output signal that indicates when data is valid and simplifies generation of CE.

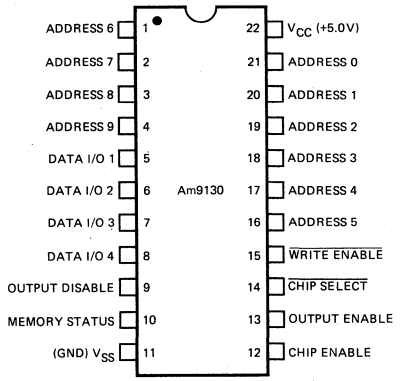
These memories may be operated in a DC standby mode for significant reductions in power dissipation. Data are retained on a deselected chip with V_{CC} as low as 1.5V.

BLOCK DIAGRAM



CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Access Time				
		500ns	400ns	300ns	250ns	200ns
Hermetic DIP	0°C to+70°C	AM9130ADC	AM9130BDC	AM9130CDC	AM9130DDC	AM9130EDC
	–55°C to +125°C	AM9130ADM	AM9130BDM	AM9130CDM		

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.25W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
Am9130XDC	$0°C \leq T_A \leq +70°C$	+5.0V ±5%	0V
Am9130XDM	$-55°C \leq T_A \leq +125°C$	+5.0V ± 10%	0V

ELECTRICAL CHARACTERISTICS over operating range (note 1)

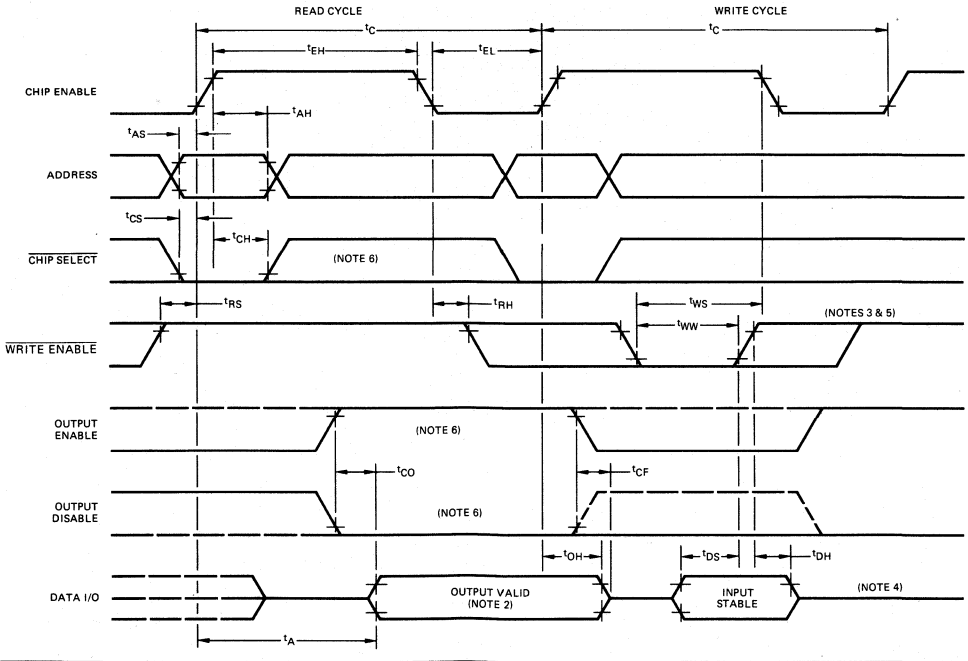
Parameters	Description	Test Conditions		Am9130XDC Min.	Am9130XDC Typ.	Am9130XDC Max.	Am9130XDM Min.	Am9130XDM Typ.	Am9130XDM Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$	$V_{CC} = 4.75V$	2.4			2.4			Volts
			$V_{CC} = 4.5V$				2.2			
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$				0.4			0.4	Volts
V_{IH}	Input HIGH Voltage			2.0		V_{CC}	2.0		V_{CC}	Volts
V_{IL}	Input LOW Voltage			−0.5		0.8	−0.5		0.8	Volts
I_{LI}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$				10			10	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$, Output disabled				10			10	μA
I_{CC}	V_{CC} Supply Current	Max. V_{CC} Output disabled	$T_A = 25°C$			120			120	mA
			$T_A = 0°C$		60	135		60	135	
			$T_A = -55°C$						150	
C_{IA}	Input Capacitance (Address)	Test frequency = 1 MHz $T_A = 25°C$ All pins at 0V			3.0	6.0		3.0	6.0	pF
C_{OUT}	Output Capacitance				4.0	7.0		4.0	7.0	pF
$C_{I/O}$	I/O Capacitance				6.0	9.0		6.0	9.0	pF
C_{IC}	Input Capacitance (Control)				6.0	9.0		6.0	9.0	pF

Notes: 1. Typical values are for $T_A = 25°C$, nominal supply voltage and nominal processing parameters.
2. The output buffer can be ON and output data valid only as long as Output Enable is HIGH and Output Disable is LOW. If either condition is changed, the output buffer will turn OFF.
3. During a write cycle, the output buffer must be turned OFF in order to eliminate conflict with input data on the I/O bus. This can be done by bringing OE LOW or bringing OD HIGH or both. It will often be convenient to tie OE to $\overline{WE}$ in order to accomplish this function. In such a case the minimum write pulse width should be longer by the output turn-off delay: $t_{WW}(min.) = t_{DS}(min.) + t_{CF}(max.)$.
4. The timing diagram specifies the input data set-up and hold times with respect to the rising edge of $\overline{WE}$. If that edge occurs during CE LOW, the data set-up is referenced to the 2.0V level of the falling edge of CE and the data hold is referenced to the 0.8V level of the falling edge of CE.
5. The minimum write pulse width specification assumes that the falling edge of $\overline{WE}$ occurs more than 50ns after the rising edge of Chip Enable. $\overline{WE}$ may fall earlier, but the minimum write pulse width requirement should be extended to compensate.
6. $\overline{CS}$, OE and OD may be operated at constant levels where appropriate. The only requirements are that $\overline{CS}$ must be HIGH to deselect the chip and either OE must be LOW or OD must be HIGH to properly perform a write operation (See Note 3).

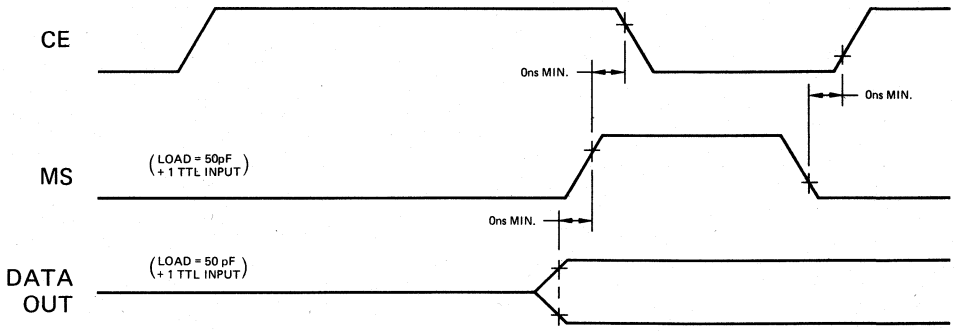
SWITCHING CHARACTERISTICS over operating range

Parameters	Description	Test Conditions	Am9130A Min.	Am9130A Max.	Am9130B Min.	Am9130B Max.	Am9130C Min.	Am9130C Max.	Am9130E Min.	Am9130E Max.	Units
t_C	Cycle Time	Transition times ≤ 20ns Output load = 1 TTL gate plus 50pF Input and output timing reference levels are 0.8V and 2.0V	840		690		530		370		ns
t_A	Access Time (CE to Output Valid Delay)		30	500	30	400	30	300	30	200	ns
t_{AS}	Address to Chip Enable Set-up Time		0		0		0		0		ns
t_{AH}	Chip Enable to Address Hold Time		200		170		130		100		ns
t_{CS}	Chip Select to Chip Enable Set-up Time		0		0		0		0		ns
t_{CH}	Chip Enable to Chip Select Hold Time		200		170		130		100		ns
t_{RS}	Read to Chip Enable Set-up Time		0		0		0		0		ns
t_{RH}	Chip Enable to Read Hold Time		0		0		0		0		ns
t_{OH}	Chip Enable to Output OFF Delay		0		0		0		0		ns
t_{DS}	Data Input Set-up Time (Note 4)		300		250		200		150		ns
t_{DH}	Data Input Hold Time (Note 4)		0		0		0		0		ns
t_{WS}	Write to Chip Enable Set-up Time		300		250		200		150		ns
t_{WW}	Write Pulse Width (Notes 3 & 5)		300		250		200		150		ns
t_{CF}	OE or OD to Output OFF Delay			210		175		135		100	ns
t_{CO}	OE or OD to Output ON Delay			250		200		150		110	ns
t_{EH}	Chip Enable HIGH Time		500		400		300		200		ns
t_{EL}	Chip Enable LOW Time		300		250		190		130		ns

SWITCHING WAVEFORMS



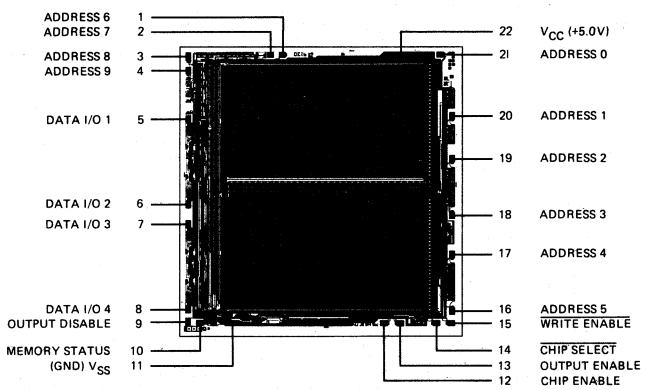
MEMORY STATUS SPECIFICATION FOR Am9130



Memory Status is an output signal from the memory indicating the real access time of the part for the operating conditions then present. It will always indicate a data access time better than the worst-case specification for the part. The exact position of MS relative to CE will change from part to part and with changing temperature and supply voltage. It will always maintain its relationship to valid output data as shown above. Nominal delay from data to MS is 15ns.

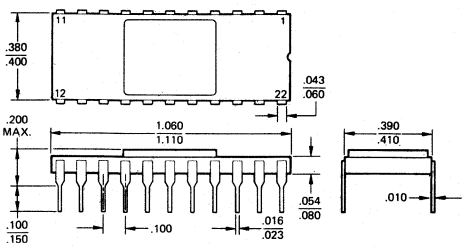
The rising edge of MS also indicates that CE may go LOW. The falling edge of MS indicates that CE may go HIGH. Thus, the MS output fully specifies the CE requirement for any part under any set of operating conditions. In fact, CE = $\overline{MS}$; the MS output may be inverted and used as the CE input. See application note for more information about the use and operation of the Memory Status signal.

Metallization and Pad Layout



DIE SIZE 0.192" x 0.197"

PHYSICAL DIMENSIONS
Dual-In-Line
22-Pin Hermetic



Am9140

4096 x 1 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- 4k x 1 organization
- Fully static data storage — no refreshing
- Single +5V power supply
- High-speed — access times down to 200ns max.
- Low-power — 710mW max. — 350mW typ.
- Interface logic levels identical to TTL
- High noise immunity — 400mV worst case
- High output drive — two standard TTL loads
- DC standby mode — reduces power by > 80%
- Uniform switching characteristics
- Dual output controls — flexible output operations
- Address and data registers on-chip
- Constant power drain — no large surges
- Unique Memory Status signal
  - —improves performance
  - —simplifies timing
- MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DESCRIPTION

The Am9140 products are high performance, low-power, 4k-bit, static, read/write random access memories. They are implemented as 4096 words by 1 bit per word. The data input and output signals use separate pins for maximum flexibility.

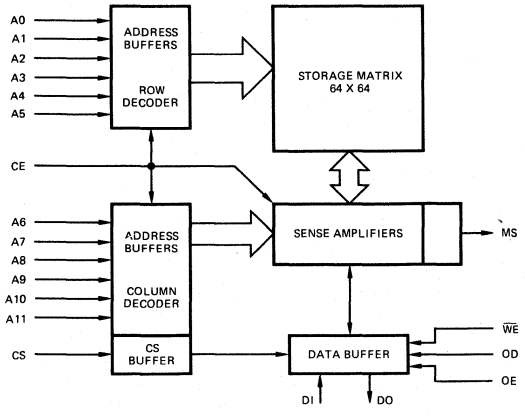
All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. The three-state output will drive two full TTL loads or eight low-power Schottky loads for increased fan-out, better capacitive drive and improved bus interface capability.

Operational cycles are initiated when the Chip Enable signal goes HIGH. When the read or write is complete, Chip Enable goes LOW to prepare the memory for the next cycle. Address and Chip Select signals are latched on-chip to help simplify system timing. Output data is also latched and is available until into the next operating cycle.

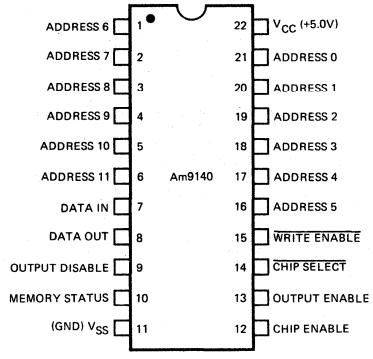
The $\overline{WE}$ signal is HIGH for all read operations and is pulsed LOW during the Chip Enable time to perform a write. Memory Status is an output signal that indicates when data is valid and simplifies generation of CE.

These memories may be operated in a DC standby mode for significant reductions in power dissipation. Data are retained on a deselected chip with V_{CC} as low as 1.5V.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Access Time				
		500ns	400ns	300ns	250ns	200ns
Hermetic DIP	0°C to +70°C	AM9140ADC	AM9140BDC	AM9140CDC	AM9140DDC	AM9140EDC
	–55°C to +125°C	AM9140ADM	AM9140BDM	AM9140CDM		

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.25W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
Am9140XDC	$0°C \leq T_A \leq +70°C$	+5.0V ±5%	0V
Am9140XDM	$-55°C \leq T_A \leq +125°C$	+5.0V ± 10%	0V

ELECTRICAL CHARACTERISTICS over operating range (note 1)

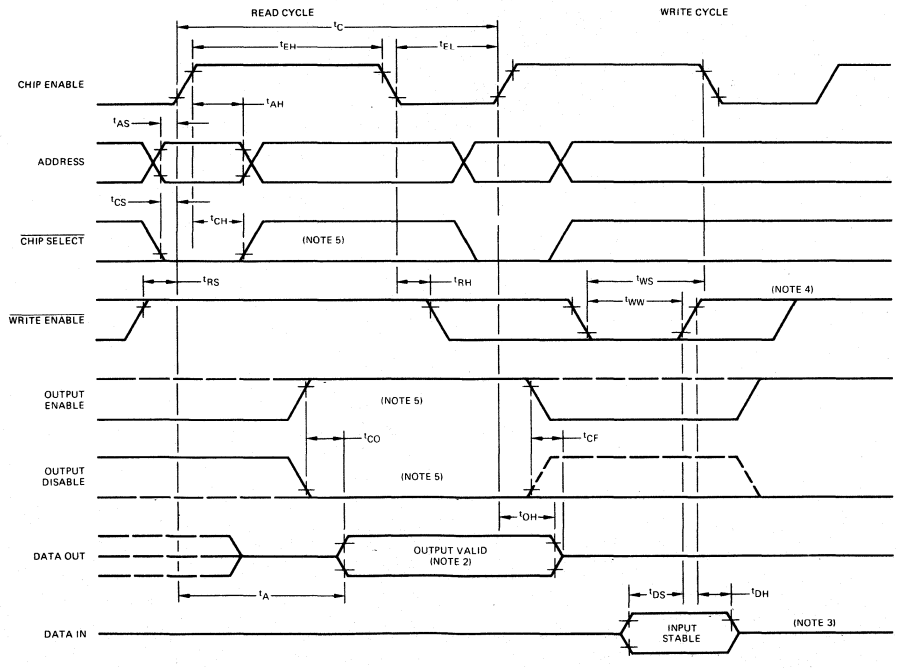
Parameters	Description	Test Conditions		Am9140XDC Min.	Am9140XDC Typ.	Am9140XDC Max.	Am9140XDM Min.	Am9140XDM Typ.	Am9140XDM Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$	$V_{CC} = 4.75V$	2.4			2.4			Volts
			$V_{CC} = 4.5V$				2.2			
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$				0.4			0.4	Volts
V_{IH}	Input HIGH Voltage			2.0		V_{CC}	2.0		V_{CC}	Volts
V_{IL}	Input LOW Voltage			−0.5		0.8	−0.5		0.8	Volts
I_{LI}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$				10			10	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$, Output disabled				10			10	μA
I_{CC}	V_{CC} Supply Current	Max. V_{CC}, Output disabled	$T_A = 25°C$			120			120	mA
			$T_A = 0°C$		60	135		60	135	
			$T_A = -55°C$						150	
C_{IA}	Input Capacitance (Address)	Test frequency = 1MHz, $T_A = 25°C$, All pins at 0V			3.0	6.0		3.0	6.0	pF
C_{OUT}	Output Capacitance				4.0	7.0		4.0	7.0	pF
C_{IC}	Input Capacitance (Control)				6.0	9.0		6.0	9.0	pF

Notes: 1. Typical values are for $T_A = 25°C$, nominal supply voltage and nominal processing parameters.
2. The output buffer can be ON and output data valid only as long as Output Enable is HIGH and Output Disable is LOW. If either condition is changed, the output buffer will turn OFF.
3. The timing diagram specifies the input data set-up and hold times with respect to the rising edge of $\overline{WE}$. If that edge occurs during CE LOW, the data set-up is referenced to the 2.0V level of the falling edge of CE and the data hold is referenced to the 0.8V level of the falling edge of CE.
4. The minimum write pulse width specification assumes that the falling edge of $\overline{WE}$ occurs more than 50ns after the rising edge of Chip Enable. $\overline{WE}$ may fall earlier, but the minimum write pulse width requirements should be extended to compensate.
5. $\overline{CS}$, OE and OD may be operated at constant levels where appropriate.

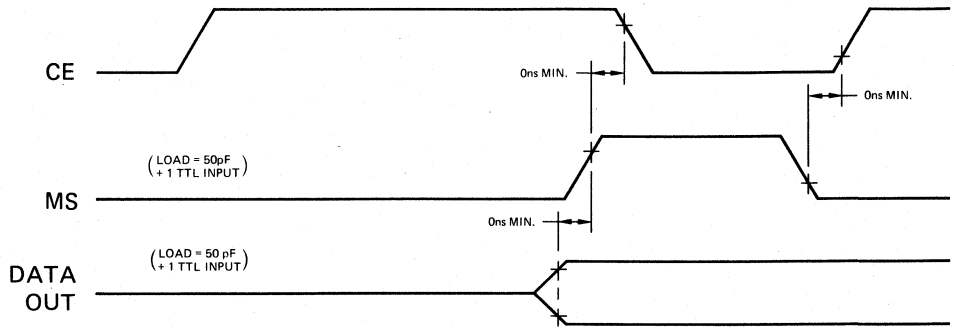
SWITCHING CHARACTERISTICS over operating range

Parameters	Description	Test Conditions	Am9140A Min.	Am9140A Max.	Am9140B Min.	Am9140B Max.	Am9140C Min.	Am9140C Max.	Am9140E Min.	Am9140E Max.	Units
t_C	Cycle Time	Transition times ≤ 20ns Output load = 1 TTL gate plus 50pF Input and output timing reference levels are 0.8V and 2.0V	840		690		530		370		ns
t_A	Access Time (CE to Output Valid Delay)		30	500	30	400	30	300	30	200	ns
t_{AS}	Address to Chip Enable Set-up Time		0		0		0		0		ns
t_{AH}	Chip Enable to Address Hold Time		200		170		130		100		ns
t_{CS}	Chip Select to Chip Enable Set-up Time		0		0		0		0		ns
t_{CH}	Chip Enable to Chip Select Hold Time		200		170		130		100		ns
t_{RS}	Read to Chip Enable Set-up Time		0		0		0		0		ns
t_{RH}	Chip Enable to Read Hold Time		0		0		0		0		ns
t_{OH}	Chip Enable to Output OFF Delay		0		0		0		0		ns
t_{DS}	Data Input Set-up Time (Note 3)		300		250		200		150		ns
t_{DH}	Data Input Hold Time (Note 3)		0		0		0		0		ns
t_{WS}	Write to Chip Enable Set-up Time		300		250		200		150		ns
t_{WW}	Write Pulse Width (Note 4)		300		250		200		150		ns
t_{CF}	OE or OD to Output OFF Delay			210		175		135		100	ns
t_{CO}	OE or OD to Output ON Delay			250		200		150		110	ns
t_{EH}	Chip Enable HIGH Time		500		400		300		200		ns
t_{EL}	Chip Enable LOW Time		300		250		200		150		ns

SWITCHING WAVEFORMS



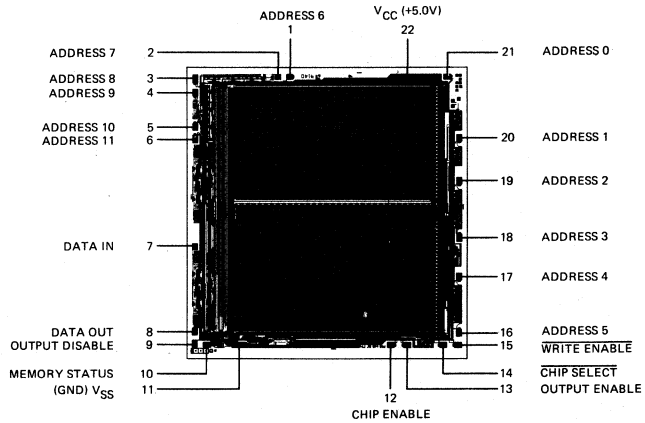
MEMORY STATUS SPECIFICATION FOR Am9140



Memory Status is an output signal from the memory indicating the real access time of the part for the operating conditions then present. It will always indicate a data access time better than the worst-case specification for the part. The exact position of MS relative to CE will change from part to part and with changing temperature and supply voltage. It will always maintain its relationship to valid output data as shown above. Nominal delay from data to MS is 15ns.

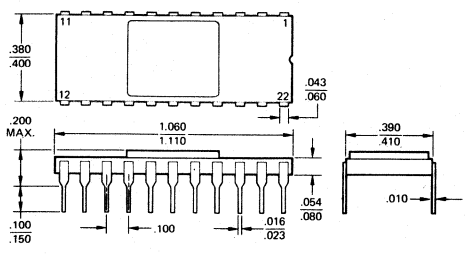
The rising edge of MS also indicates that CE may go LOW. The falling edge of MS indicates that CE may go HIGH. Thus, the MS output fully specifies the CE requirement for any part under any set of operating conditions. In fact, CE = $\overline{MS}$; the MS output may be inverted and used as the CE input. See application note for more information about the use and operation of the Memory Status signal.

Metallization and Pad Layout



DIE SIZE 0.192" x 0.197"

PHYSICAL DIMENSIONS
Dual-In-Line
22-Pin Hermetic



Am9101/Am91L01/Am2101 FAMILY

256x4 Static R/W Random Access Memories

PART NUMBER	Am2101	Am2101-2	Am9101A Am91L01A Am2101-1	Am9101B Am91L01B	Am9101C Am91L01C	Am9101D	Am9101E
ACCESS TIME	1000ns	650ns	500ns	400ns	300ns	250ns	200ns

DISTINCTIVE CHARACTERISTICS

- 256 x 4 organization
- Low operating power
  125mW Typ; 290mW maximum — standard power
  100mW Typ; 175mW maximum — low power
- DC standby mode reduces power up to 84%
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads
- High noise immunity — full 400mV
- Single 5 volt power supply —
  tolerances: ±5% commercial, ±10% military
- Uniform switching characteristics — access times insensitive to supply variations, addressing patterns and data patterns
- Both military and commercial temperature ranges available
- Two chip enable inputs
- Output disable control
- Zero address set-up and hold times for simplified timing
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DESCRIPTION

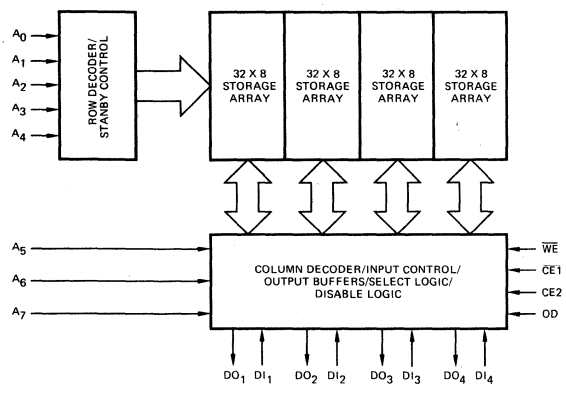
The Am9101/Am91L01 series of devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

These memories may be operated in a DC standby mode for reductions of as much as 84 percent of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L01 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the stand-by mode.

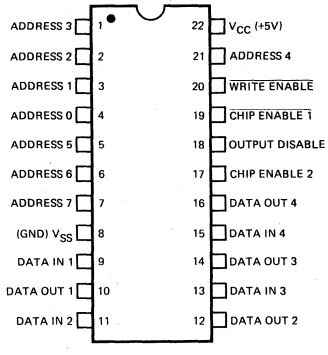
The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are all fully static and no refresh operations or sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

Am9101 BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Flat Pack version available in 24-pin package.
See page 4 for pin configuration.

ORDERING INFORMATION

AMBIENT TEMPERATURE SPECIFICATION	PACKAGE TYPE	POWER TYPE	ACCESS TIMES						
			1000ns	650ns	500ns	400ns	300ns	250ns	200ns
0°C to +70°C	Molded DIP	Standard	P2101	P2101-2	P2101-1 AM9101APC	AM9101BPC	AM9101CPC	AM9101DPC	AM9140PC
		Low			AM91L01APC	AM91L01BCP	AM91L01CPC		
	Hermetic DIP	Standard	C2101	C2101-2	C2101-1 AM9101ADC	AM9101BDC	AM9101CDC	AM9101DDC	AM9140EDC
		Low			AM91L01ADC	AM91L01BDC	AM91L01CDC		
−55°C to +125°C	Hermetic DIP	Standard			AM9101ADM	AM9101BDM	AM9101CDM		
		Low			AM91L01ADM	AM91L01BDM	AM91L01CDM		
	Hermetic Flat Pack	Standard			AM9101AFM	AM9101BFM			
		Low			AM91L01AFM	AM91L01BFM			

Am9102/Am91L02 FAMILY

1024x1 Static R/W Random Access Memories

DISTINCTIVE CHARACTERISTICS

- Low-Power Dissipation
  100 mW typical; 260 mW maximum
- Standby operating mode reduces power 84%
  18 mW typical; 42 mW maximum
- Input and output voltage levels identical to TTL
- High-Output Drive – Two full TTL loads guaranteed
- High Noise Immunity – 400 mV guaranteed
- Uniform Access Times
  Switching characteristics are insensitive to data patterns, addressing patterns, and power supply variations
- Single 5-Volt Power Supply
  10% tolerance for full temperature range devices
  5% tolerance for commercial range devices
- High-Performance Plug-In Replacement for: Intel 2102, Signetics 2602, Intersil IM7552, Mostek 4102, TI4033/4/5
- Available for operation over both commercial and military ranges
- 100% reliability assurance testing in accordance with MIL-STD-883
- Zero data hold and address hold times simplify timing requirements

FUNCTIONAL DESCRIPTION

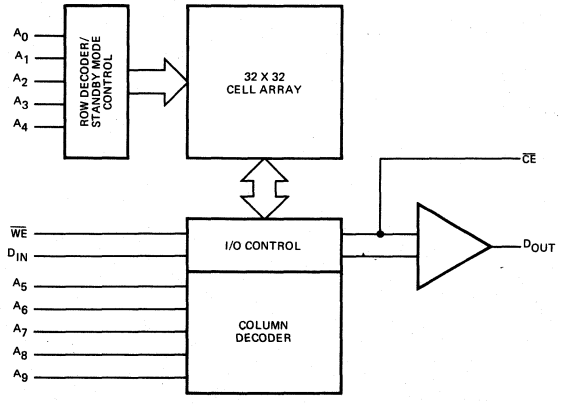
The Am9102 Family of 1024-bit static N-channel RAMs contains members with cycle times ranging from 650ns to 200ns All the devices are organized as 1024 x 1, and all have a power-saving standby operating mode.

Each device has a chip enable input (CE) that controls a three-state output to make construction of large memory systems simple. Reading and writing are performed by enabling the chip and applying a LOW to write or a HIGH to read on the write enable input ($\overline{WE}$). All inputs are directly TTL compatible with no external components required, and the output will drive two full TTL loads in both the HIGH and LOW states.

The devices operate from a single +5 volt power supply. The power dissipation of the devices can be reduced to about 16% of the normal operating power by lowering the voltage on the power supply pin. Data is guaranteed to be retained in the power-down condition.

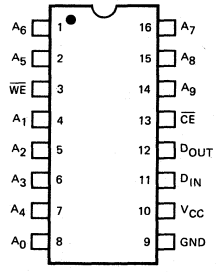
All unit members in the family are available in plastic or hermetic DIPs for operation over the commercial temperature range and, except for the Am9102D/E, may all also be purchased for operation over the military temperature range. All AC and DC parameters are guaranteed over the operating range.

BLOCK DIAGRAM



CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

AMBIENT TEMPERATURE	PACKAGE TYPE	POWER TYPE	ACCESS TIMES					
			650ns	500ns	400ns	300ns	250ns	200ns
0°C ≤ T_A ≤ +70°C	Molded DIP	Standard	AM9102PC	AM9102APC	AM9102BPC	AM9102CPC	AM9102DPC	Am9102EPC
		Low	AM91L02PC	AM91L02APC	AM91L02BPC	AM91L02CPC		
	Hermetic DIP	Standard	AM9102DC	AM9102ADC	AM9102BDC	AM9102CDC	AM9102DDC	Am9102EDC
		Low	AM91L02DC	AM91L02ADC	AM91L02BDC	AM91L02CDC	AM91L01CDC	
−55°C to +125°C	Hermetic DIP	Standard	AM9102DM	AM9102ADM	AM9102BDM	AM9102CDM	AM9101CDM	
		Low	AM91L02DM	AM91L02ADM	AM91L02BDM	AM91L02CDM	AM91L01CDM	
	Hermetic Flat Pack	Standard	AM9102FM	AM9102AFM	AM9102BFM			
		Low	AM91L02FM	AM91L02AFM	AM91L02BFM			

Am9111/Am91L11/Am2111 FAMILY

256x4 Static R/W Random Access Memories

PART NUMBER	Am2111	Am2111-2	Am9111A Am91L11A Am2111-1	Am9111B Am91L11B	Am9111C Am91L11C	Am9111D	AM9111E
ACCESS TIME	1000ns	650ns	500ns	400ns	300ns	250ns	200ns

DISTINCTIVE CHARACTERISTICS

- 256 x 4 organization for small memory systems
- Low operating power dissipation
  125mW Typ; 290mW maximum — standard power
  100mW Typ; 175mW maximum — low power
- DC standby mode reduces power up to 84%
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads
- High noise immunity — full 400mV
- Single 5 volt power supply —
  tolerances: ±5% commercial, ±10% military
- Uniform switching characteristics — access times insensitive to supply variations, addressing patterns and data patterns
- Both military and commercial temperature ranges available
- Bussed input and output data on common pins.
- Output disable control
- Zero address set-up and hold times for simplified timing
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DESCRIPTION

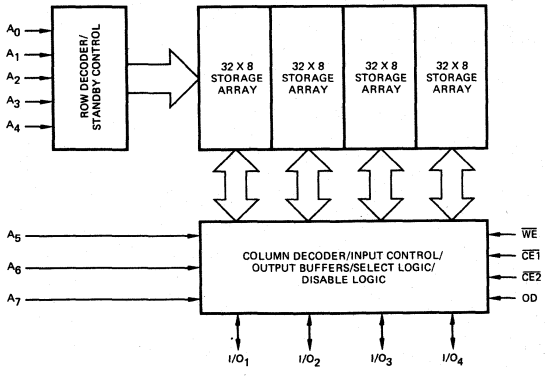
The Am9111/Am91L11 series of devices are high performance, low power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth. The input data and output data signals are bussed together to share common I/O pins. This feature not only decreases the package size, but helps eliminate external logic in bus-oriented memory systems.

These memories may be operated in a DC standby mode for reductions of as much as 84% of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L11 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the stand-by mode.

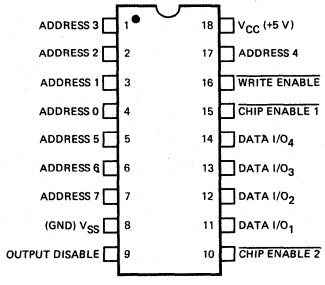
The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are all fully static and no refresh operations or sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

Am9111 BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Flat Pack version available in 24-pin package.
See page 4 for pin configuration.

ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Power Type	Access Times						
			1000ns	650ns	500ns	400ns	300ns	250ns	200ns
0°C to +70°C	Molded DIP	Standard	P2111	P2111-2	P2111-1 AM9111APC	AM9111BPC	AM9111CPC	AM9111DPC	AM9111EPC
		Low			AM91L11APC	AM91L11BPC	AM91L11CPC		
	Hermetic DIP	Standard	C2111	C2111-2	C2111-1 AM9111ADC	AM9111BDC	AM9111CDC	AM9111DDC	AM9111EDC
		Low			AM91L11ADC	AM91L11BDC	AM91L11CDC		
−55°C to +125°C	Hermetic DIP	Standard			AM9111ADM	AM9111BDM	AM9111CDM		
		Low			AM91L11ADM	AM91L11BDM	AM91L11CDM		
	Hermetic Flat Pack	Standard			AM9111AFM	AM9111BFM			
		Low			AM91L11AFM	AM91L11BFM			

Am9112/Am91L12 FAMILY

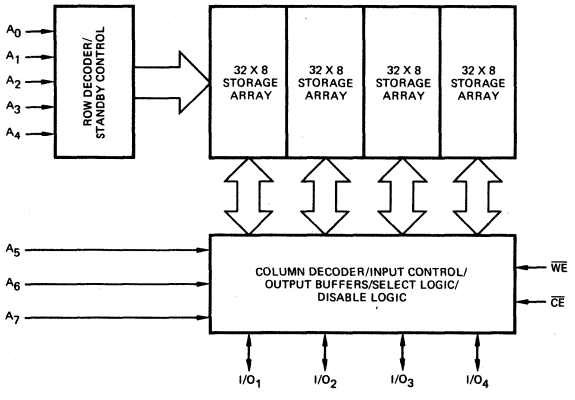
256x4 Static R/W Random Access Memories

Part Number	Am2112	Am2112-2	Am9112A Am91L12A	Am9112B Am91L12B	Am9112C Am91L12C	Am9112D	AM9112E
Access Time	1000ns	650ns	500ns	400ns	300ns	250ns	200ns

Distinctive Characteristics

- 256 x 4 organization
- 16-pin standard DIP
- Low operating power dissipation
  125mW Typ; 290mW maximum — standard power
  100mW Typ; 175mW maximum — low power
- DC standby mode reduces power up to 84%
  20mW Typ; 47mW maximum
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads guaranteed
- High noise immunity — full 400mV
- Uniform switching characteristics — access times insensitive to supply variations, address patterns and data patterns.
- Single +5V power supply — tolerances ±5% commercial, ±10% military
- Bus oriented I/O data
- Zero address, set-up, and hold times guaranteed for simpler timing
- Direct plug-in replacement for 2112 type devices
- 100% MIL-STD-883 reliability assurance testing

Am9112 BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The Am9112/Am91L12 series of products are high performance, low power, 1024-bit, static read/write random access memories. They offer a range of speeds and power dissipations including versions as fast as 200ns and as low as 100mW typical.

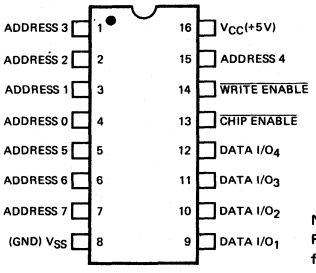
Each memory is implemented as 256 words by 4-bits per word. This organization allows efficient design of small memory systems and permits finer resolution of incremental memory word size relative to 1024 by 1 devices. The output and input data signals are internally bussed together and share 4 common I/O pins. This feature keeps the package size small and provides a simplified interface to bus-oriented systems.

The Am9112/Am91L12 memories may be operated in a DC standby mode for reductions of as much as 84% of the normal operating power dissipation. Though the memory cannot be operated, data can be retained in the storage cells with a power supply as low as 1.5 volts. The Am91L12 versions offer reduced power during normal operating conditions as well as even lower dissipation in standby mode.

The eight Address inputs are decoded to select 1-of-256 locations within the memory. The Chip Enable input acts as a high-order address in multiple chip systems. It also controls the write amplifier and the output buffers in conjunction with the Write Enable input. When $\overline{CE}$ is low and $\overline{WE}$ is high, the write amplifiers are disabled, the output buffers are enabled and the memory will execute a read cycle. When $\overline{CE}$ is low and $\overline{WE}$ is low, the write amplifiers are enabled, the output buffers are disabled and the memory will execute a write cycle. When $\overline{CE}$ is high both the write amplifiers and the output buffers are disabled.

These memories are fully static and require no refresh operations or sense amplifiers or clocks. All input and output voltage levels are identical to standard TTL specifications, including the power supply.

CONNECTION DIAGRAM
Top View



Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Power Type	Access Time						
			1000ns	650ns	500ns	400ns	300ns	250ns	200ns
0°C to +70°C	Molded DIP	Standard	P2112	P2112-2	AM9112APC	AM9112BPC	AM9112CPC	AM9112DPC	AM9112EPC
		Low			AM91L12APC	AM91L12BPC	AM91L12CPC		
	Hermetic DIP	Standard	C2112	C2112-2	AM9112ADC	AM9112BDC	AM9112CDC	AM9112DDC	AM9112EDC
		Low			AM91L12ADC	AM91L12BDC	AM91L12CDC		
−55°C to +125°C	Hermetic DIP	Standard			AM9112ADM	AM9112BDM	AM9112CDM		
		Low			AM91L12ADM	AM91L12BDM	AM91L12CDM		
	Hermetic Flat Pack	Standard			AM9112AFM	AM9112BFM			
		Low			AM91L12AFM	AM91L12BFM			

PRODUCT ASSURANCE
MIL-M-38510 • MIL-Q-9858A • MIL-STD-883

The product assurance program at Advanced Micro Devices defines manufacturing flow, establishes standards and controls, and confirms the product quality at critical points. Standardization under this program assures that all products meet military and government agency specifications for reliable ground applications. Further screening for users desiring flight hardware and other higher reliability classes is simplified because starting product meets all initial requirements for high-reliability parts.

The quality standards and screening methods of this program are equally valuable for commercial parts where equipment must perform reliably with minimum field service.

Three military documents provide the foundation for this program. They are:

MIL-M-38510—General Specification for Microcircuits
MIL-Q-9858—Quality Program Requirements
MIL-STD-883—Test Methods and Procedures for Microelectronics

MIL-M-38510 describes design, processing and assembly workmanship guidelines for military and space-grade integrated circuits. **All linear, MSI, and computer interface circuits manufactured by Advanced Micro Devices for full temperature range (−55°C to +125°C) operation meet these quality requirements of MIL-M-38510.**

MIL-Q-9858 identifies 28 elements of management, planning and control that are necessary in maintaining a quality program. **Advanced Micro Devices complies with all requirements of MIL-Q-9858.**

MIL-STD-883 contains detail testing and inspection methods for integrated circuits. Three of the methods are quality and processing standards directly related to product assurance:

Test Method 2010 defines the visual inspection of integrated circuits before sealing. By confirming fabrication and assembly quality, inspection to this standard assures the user of reliable circuits in long-term field applications. Standard inspection at Advanced Micro Devices includes all the requirements of Method 2010, condition B.

Test Method 5004 defines three reliability classes of parts. All must receive certain basic inspection, preconditioning and screening stresses. The classes are:

Class C — Used where replacement can be readily accomplished. Screening steps are given in the AMD processing flow chart.

Class B — Used where maintenance is difficult or expensive and where reliability is vital. Devices are upgraded from Class C to Class B by 160-hour burn-in at 125°C. All other process requirements are the same.

Class A — Used where replacement is extremely difficult and reliability is imperative. Class A screening selects extra reliability parts by expanded visual and X-ray inspection, further burn-in, and tighter sampling inspection.

All hermetically sealed integrated circuits (military and commercial) manufactured by Advanced Micro Devices are screened to Class C. Electrical burn-in upgrades any product to a full Class B screened part on a short delivery cycle.

All molded integrated circuits receive Class C screening except that centrifuge and hermeticity steps are omitted for solid-package parts.

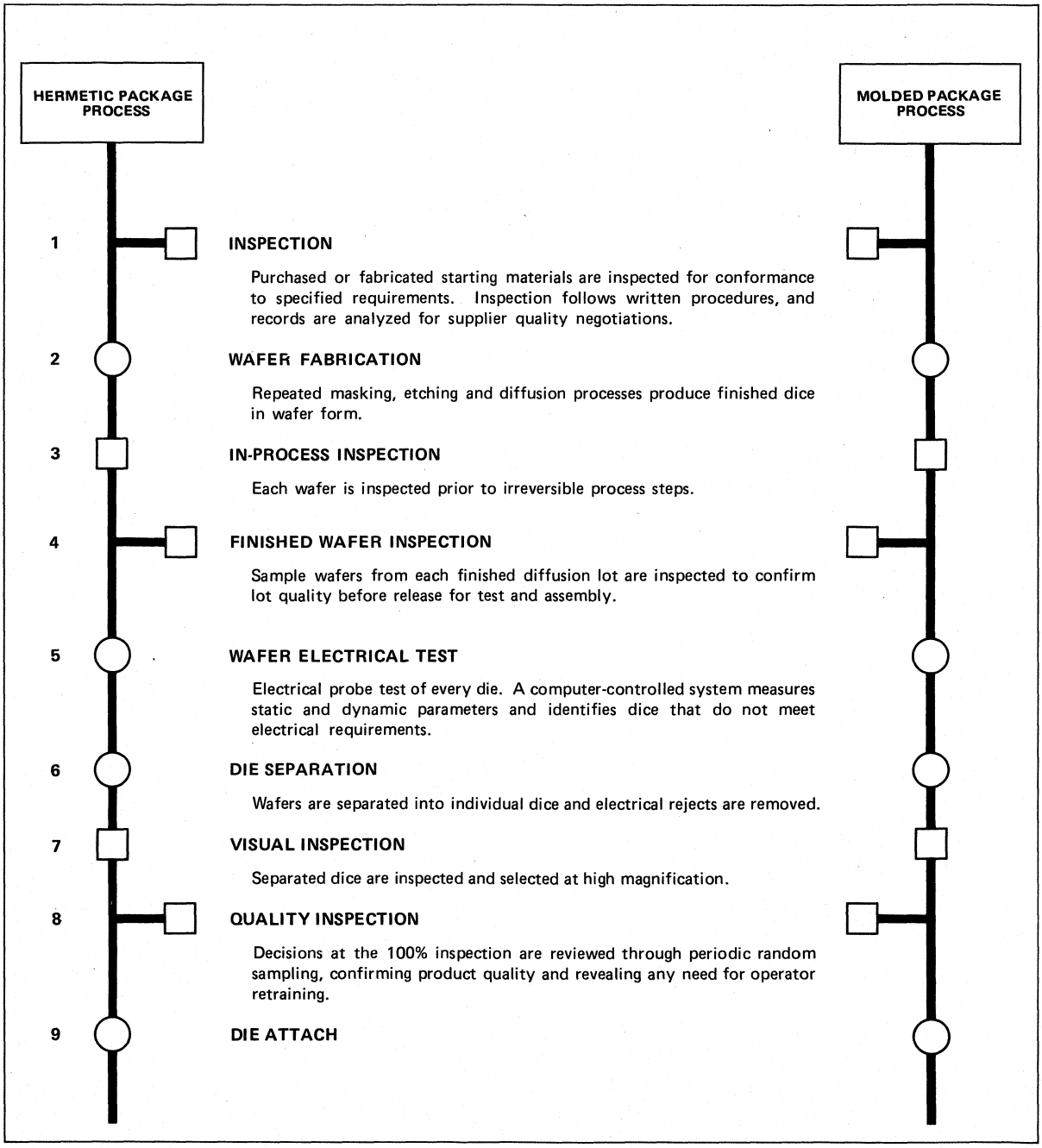
Test Method 5005 defines qualification and quality conformance procedures. Subgroups, tests and quality levels for each class are given for Group A (electrical), Group B (mechanical quality measurements related to the user's assembly environment), and Group C (long-term reliability and product design stress tests). Group A tests are always performed; Group B and C may be specified by the user. Tables I, II, and III give standard test groupings and quality levels for Class B screened devices. These quality levels are used as a minimum for all tests.

MANUFACTURING, SCREENING AND INSPECTION FOR INTEGRATED CIRCUITS

All integrated circuits are screened to MIL-STD-883, Method 5004, Class C; quality conformance inspection where required is performed to Class B levels.

All full-temperature-range (−55°C to +125°C) linear, MSI and computer-interface circuits are manufactured to the workmanship requirements of MIL-M-38510.

The flow chart identifies processing steps as they relate to MIL-STD-883 and MIL-M-38510.



10 **QUALITY INSPECTION**

Strength of die attachment, position of die and visual quality of eutectic wetting are confirmed periodically by inspecting random samples and push-testing the attached dice.

11 **WIRE BOND**

Hermetic: Aluminum wires, ultrasonic bonding.
Molded: Gold wires, thermocompression bonding.

12 **QUALITY INSPECTION**

Weld strength, bond size and position, wire dress and general workmanship are confirmed periodically by comparing random samples with assembly instructions and quality standards. Bond strength is plotted on statistical control charts, providing early warning of process drifts.

13 **INTERNAL VISUAL INSPECTION**

Assembled but unsealed units are individually inspected at low and high power.

QUALITY STANDARDS:

All devices—MIL-STD-883, Method 2010, Condition B.
Full temperature devices identified above—MIL-M-38510, Para. 3.7 for workmanship.

14 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, providing confirmation of product quality and revealing any need for operator retraining.

15a **FINAL SEAL**

(Hermetic devices)

15b **ENCAPSULATE**

(Molded Devices)

16 **STABILIZATION BAKE**

MIL-STD-883, Method 1008, Cond. C: 150°C, 24 hr

17 **TEMPERATURE CYCLE**

MIL-STD-883, Method 1010, Cond. C: −65°C, +150°C, 10 cycles

18 **CENTRIFUGE**

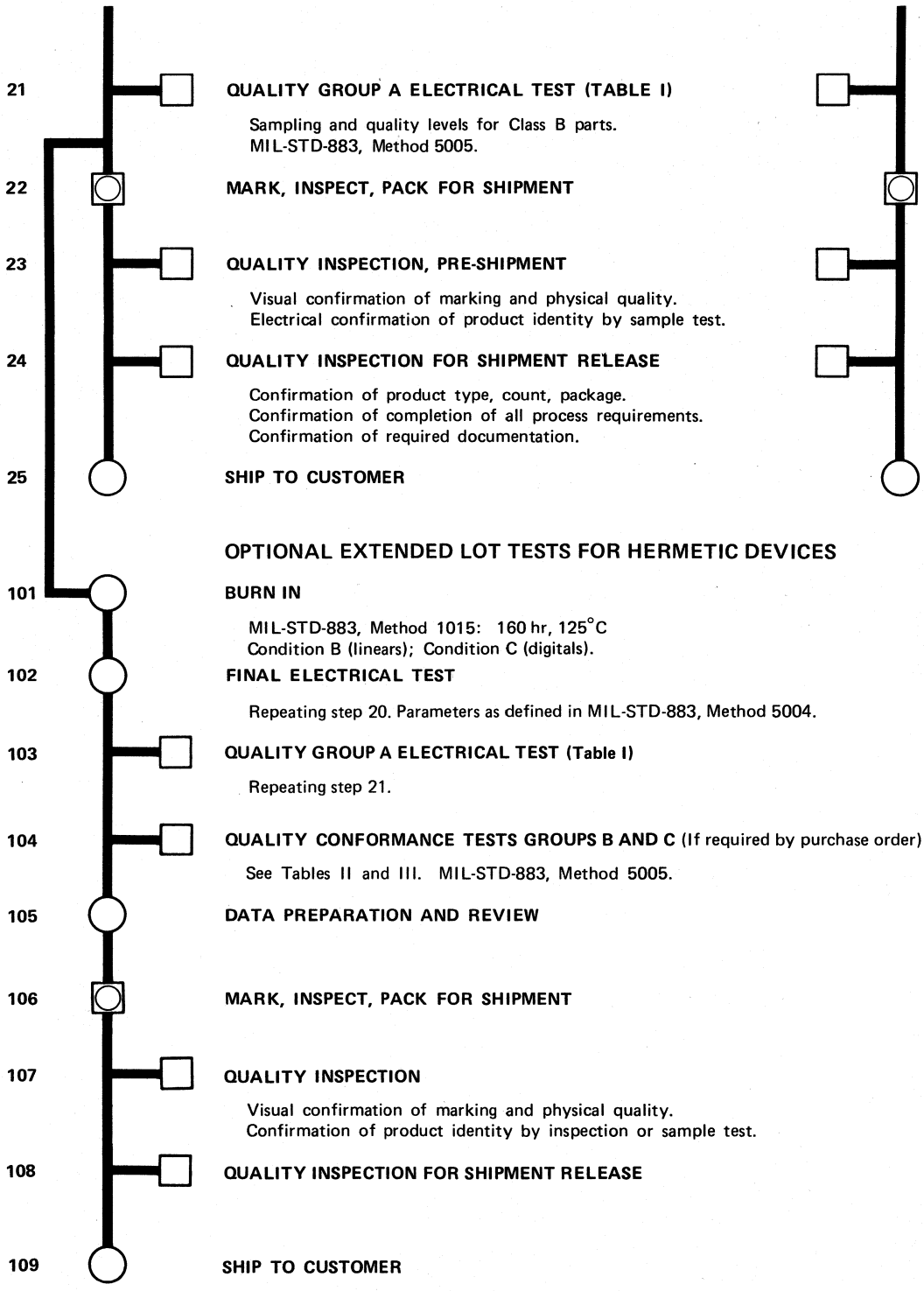
MIL-STD-883, Method 2001, Cond. E: 30,000 G

19 **SEAL**

MIL-STD-883, Method 1014, Cond. A or B: Fine Leak
MIL-STD-883, Method 1014, Cond. C2: Gross Leak

20 **ELECTRICAL TEST**

MIL-STD-883, Method 5004, Para. 3.1.12: Static, dynamic, functional tests at 25°C.



21 **QUALITY GROUP A ELECTRICAL TEST (TABLE I)**

Sampling and quality levels for Class B parts.
MIL-STD-883, Method 5005.

22 **MARK, INSPECT, PACK FOR SHIPMENT**

23 **QUALITY INSPECTION, PRE-SHIPMENT**

Visual confirmation of marking and physical quality.
Electrical confirmation of product identity by sample test.

24 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Confirmation of product type, count, package.
Confirmation of completion of all process requirements.
Confirmation of required documentation.

25 **SHIP TO CUSTOMER**

OPTIONAL EXTENDED LOT TESTS FOR HERMETIC DEVICES

101 **BURN IN**

MIL-STD-883, Method 1015: 160 hr, 125°C
Condition B (linears); Condition C (digitals).

102 **FINAL ELECTRICAL TEST**

Repeating step 20. Parameters as defined in MIL-STD-883, Method 5004.

103 **QUALITY GROUP A ELECTRICAL TEST (Table I)**

Repeating step 21.

104 **QUALITY CONFORMANCE TESTS GROUPS B AND C** (If required by purchase order)

See Tables II and III. MIL-STD-883, Method 5005.

105 **DATA PREPARATION AND REVIEW**

106 **MARK, INSPECT, PACK FOR SHIPMENT**

107 **QUALITY INSPECTION**

Visual confirmation of marking and physical quality.
Confirmation of product identity by inspection or sample test.

108 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

109 **SHIP TO CUSTOMER**

QUALIFICATION AND QUALITY CONFORMANCE INSPECTION

Subgroups and LTPD levels as given in MIL-STD-883A, Method 5005.2, for Class B parts. We will revise these tests accordingly whenever MIL-STD-883 is revised. The latest revision of each test method is used.

Table I. Group A Electrical Tests

Subgroups**	LTPD	Initial Sample Size*
Subgroup 1 – Static tests at 25°C	5	45
Subgroup 2 – Static tests at maximum rated operating temperature	7	32
Subgroup 3 – Static tests at minimum rated operating temperature	7	32
Subgroup 4 – Dynamic tests at 25°C	5	45
Subgroup 5 – Dynamic tests at maximum rated operating temperature	7	32
Subgroup 6 – Dynamic tests at minimum rated operating temperature	7	32
Subgroup 7 – Functional tests at 25°C	5	45
Subgroup 8 – Functional tests at maximum and minimum rated operating temperatures	10	22
Subgroup 9 – Switching tests at 25°C	7	32

* See footnote following Table III.
** If Group A Subgroups are combined, the tightest LTPD will apply to the total of tests.

Table II. Group B Tests

Test	Method	Conditions	LTPD	Initial Sample Size*
Subgroup 1 Physical dimensions	2016	AMD standard dimensions unless listed by customer	15	15
Subgroup 2 a) Resistance to Solvents	2015	Alcohol, mineral spirits, trichloroethane, and Freon solvents	3 devices	
b) Internal visual and mechanical	2014		1 device	
c) Bond strength	2011	Test Condition D: Force limits per Method 2011.	15	15 leads
Subgroup 3 Solderability	2003	Soldering temperature 260°C ±10°C	15	15 leads
Subgroup 4 a) Lead integrity	2004	Test Condition B2: 3 oz for ribbon leads; 8 oz for all others.	15	15
b) Seal 1. Fine leak 2. Gross leak	1014 1014	Cond A: Helium, or Cond B: Radioactive Tracer Cond C, Step 2: Fluorocarbon		

Table III. Group C tests

Test	Method	Conditions	LTPD	Initial Sample Size*
Subgroup 1				
a) Thermal shock	1011	Test Condition B: liquid to liquid, 125°C to −55°C , 15 cycles		
b) Temperature cycling	1010	Test Condition C: air to air, −65°C to +150°C, 10 cycles	15	15
c) Moisture resistance	1004	Omit initial conditioning and vibration		
d) Seal (fine and gross)	1014			
e) Visual examination				
f) End point electrical test		DC room temperature parameters		
Subgroup 2				
a) Mechanical shock	2002	Test Condition B: 5 shock pulses; 6 directions; 1,500 G		
b) Vibration variable frequency	2007	Test Condition A: 20 Hz-2 KHz; 20 G, X, Y, Z orientation	15	15
c) Constant acceleration (Centrifuge)	2001	Test Condition E: 30 KG centrifugal acceleration		
d) Seal (fine and gross)	1014			
e) Visual examination				
f) End point electrical test		DC room temperature parameters		
Subgroup 3				
a) Salt atmosphere	1009	Test Condition A: 24 hr	15	15
b) Visual examination				
Subgroup 4				
a) High Temperature storage	1008	Test Condition C: 1,000 hr, 150°C	7	55 Acc = 1*
b) End point electrical test		DC room temperature parameters		
Subgroup 5				
a) Operating life test	1005	Steady state power: 1000 hr, 125°C. Digital devices: Test Condition C Linear devices: Test Condition B	5	77 Acc = 1*
b) End point electrical test		DC room temperature parameters		

* Groups A, B and C sampling plans are based on standard LTPD tables of MIL-M-38510. The smallest sample size, based on zero rejects allowed, has otherwise indicated. If necessary, the sample size will be increased once to the quantity not exceeding an acceptance number of 3 for Group A and 2 for Groups B and C.

End point electrical parameters, where required, are room temperature DC and functional tests.

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